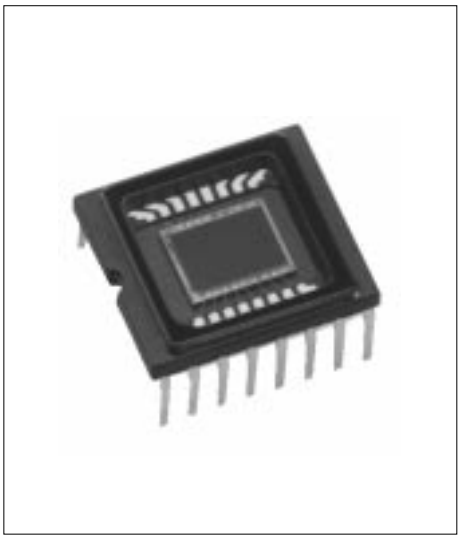
MN3726FT,MN3726AT

6mm (type-1/3) 512H High-Resposivity CCD Area Image Sensors



■ Overview

The MN3726FT and MN3726AT are 6mm (type-1/3) interline transfer CCD (IT-CCD) solid state image sensor devices.

This device uses photodiodes in the optoelectric conversion section and CCDs for signal read out. The electronic shutter function has made an exposure time of 1/10000 seconds possible. Further, this device has the features of high sensitivity, low noise, broad dynamic range, and low smear.

This device has a total of 316,528 pixels (542 horizontal × 584 vertical) and provides stable and clear images with a resolution of 330 horizontal TV-lines and 420 vertical TV-lines.

Part Number	Size	System	Color or B/W
MN3726FT	6mm(type-1/3)	PAL	Color
MN3726AT		CCIR	B/W

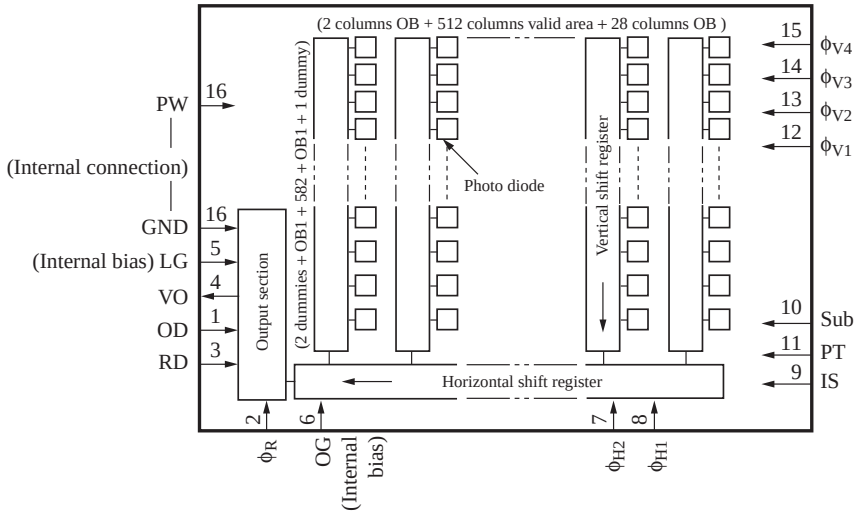
■ Features

- Total number of pixels: 542 (horizontal) × 584 (vertical)
- High sensitivity
- Low noise
- Broad dynamic range
- Low smear
- Low image lag
- Electronic shutter
- No image distortion
- Small size enables design of compact equipment
- High reliability
- 16-pin DIL plastic package

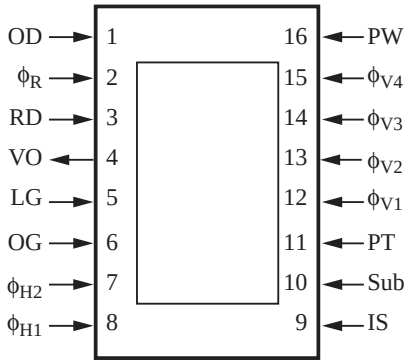
■ Applications

- Compact lightweight camcorders
- Communication television systems
- Door cameras
- Cameras for measurement, and medical use

■ Block Diagram



■ Pin Assignments



(Top View)

■ Pin Descriptions

Pin No.	Symbol	Descriptions	Pin No.	Symbol	Descriptions
1	OD	Output drain	11	PT	P-well for protection circuit
2	ϕ_R	Reset pulse	12	ϕ_{V1}	Vertical shift register clock pulse 1
3	RD	Reset drain			
4	VO	Video output	13	ϕ_{V2}	Vertical shift register clock pulse 2
5	LG	Output load transistor gate			
6	OG	Output gate	14	ϕ_{V3}	Vertical shift register clock pulse 3
7	ϕ_{H2}	Horizontal register clock pulse 2			
8	ϕ_{H1}	Horizontal register clock pulse 1	15	ϕ_{V4}	Vertical shift register clock pulse 4
9	IS	Horizontal CCD input source			
10	Sub	Substrate	16	PW	P-well

■ Absolute Maximum Ratings and Operating Conditions

Parameter		Symbol	Rating		Operating condition			Unit
			min	max	min	typ	max	
Reset drain voltage		V_{RD}	– 0.2	18.0	14.5	15.0	15.5	V
Output drain voltage		V_{OD}	– 0.2	18.0	14.5	15.0	15.5	V
Output load transistor gate voltage		V_{LG}	Supplied internally					V
Output gate voltage		V_{OG}	Supplied internally					V
Horizontal CCD input source voltage		V_{HS}	– 0.2	18.0	14.5	15.0	15.5	V
Protection P-well voltage		V_{PT} *2	– 10.0	0.2	$\phi_{V(L)}$ – 1.2	$\phi_{V(L)}$ – 1.0	$\phi_{V(L)}$ – 0.7	V
P-well voltage		V_{PW}	Reference voltage		—	0	—	V
Reset pulse voltage	H-L	$V_{\phi R(H-L)}$ *3	—	18.0	4.7	5.0	5.3	V
	Bias	$V_{\phi R(Bias)}$ *3	– 0.2	—	0	Adjust	5.0	V
Horizontal register clock pulse voltage 2		$V_{\phi H1(H)}$	—	18.0	4.5	5.0	5.5	V
		$V_{\phi H1(L)}$	– 0.2	—	– 0.1	0	0.1	
Horizontal register clock pulse voltage 2		$V_{\phi H2(H)}$	—	18.0	4.5	5.0	5.5	V
		$V_{\phi H2(L)}$	– 0.2	—	– 0.1	0	0.1	
Vertical shift register clock pulse voltage 1		$V_{\phi V1(H)}$ *2	—	18.0	14.5	15.0	15.5	V
		$V_{\phi V1(M)}$ *2	—	—	– 0.2	0	0.2	
		$V_{\phi V1(L)}$ *2	– 9.0	—	– 7.3	– 7.0	– 6.7	
Vertical shift register clock pulse voltage 2		$V_{\phi V2(M)}$ *2	—	15.0	0.8	1.0	1.2	V
		$V_{\phi V2(L)}$ *2	– 9.0	—	– 7.3	– 7.0	– 6.7	
Vertical shift register clock pulse voltage 3		$V_{\phi V3(H)}$ *2	—	18.0	14.5	15.0	15.5	V
		$V_{\phi V3(M)}$ *2	—	—	– 0.2	0	0.2	
		$V_{\phi V3(L)}$ *2	– 9.0	—	– 7.3	– 7.0	– 6.7	
Vertical shift register clock pulse voltage 4		$V_{\phi V4(M)}$ *2	—	15.0	0.8	1.0	1.2	V
		$V_{\phi V4(L)}$ *2	– 9.0	—	– 7.3	– 7.0	– 6.7	
Substrate voltage		V_{Sub} *1	– 0.2	45.0	3.0	Adjust	13.8	V
		ϕV_{Sub} *4	—	—	24.5	25.0	25.5	
Operating temperature		T_{opr}	– 10	70	—	25	—	°C
Storage temperature		T_{stg}	– 30	80	—	—	—	°C

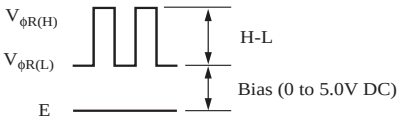
Note) 1. Standard light input defines

Standard light input is the one when the exposure is done at a lens aperture of F8, using a light source of 2856 K and 1050 nt, and placing a color temperature conversion filter LB-40 (HOYA) and an IR cutting filter CAW-500 (t = 2.5 mm) in the light path.

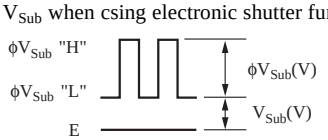
2. *1: V_{Sub} internal settings guarantee blooming at 400 times light input of the standard light input.
3. *2: V_{PT} is set so that the following conditions are set for VL of the vertical shift clock.

$V_{PT} \leqq VL$

4. *3:



5. *4: V_{Sub} when csing electronic shutter function

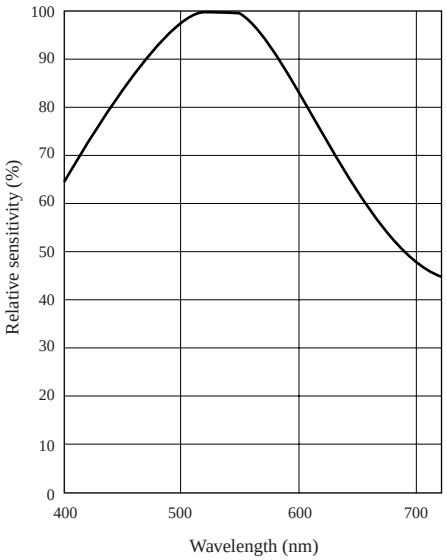


■ Optical Characteristics

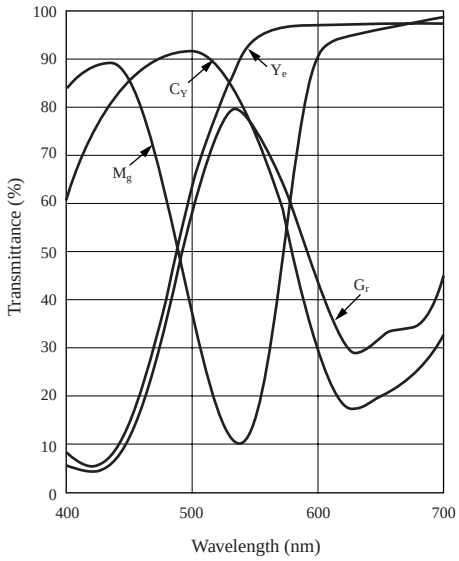
Part Number	Color or B/W	Effective pixels H	Effective pixels V	S/N typ (dB)	Saturation output typ (mV)	Sensitivity F8 typ (mV)	Vertical smear Sm typ(%)	Image lag typ (%)	Horizontal resolution typ (TV-lines)	Vertical resolution typ (TV-lines)
MN3726FT	Color	512	582	—	900	350	0.002	—	330	420
MN3726AT	B/W	512	582	—	1,500	500	0.003	—	360	420

■ Graphs of Characteristics

CCD Spectral Characteristics (without color filter)

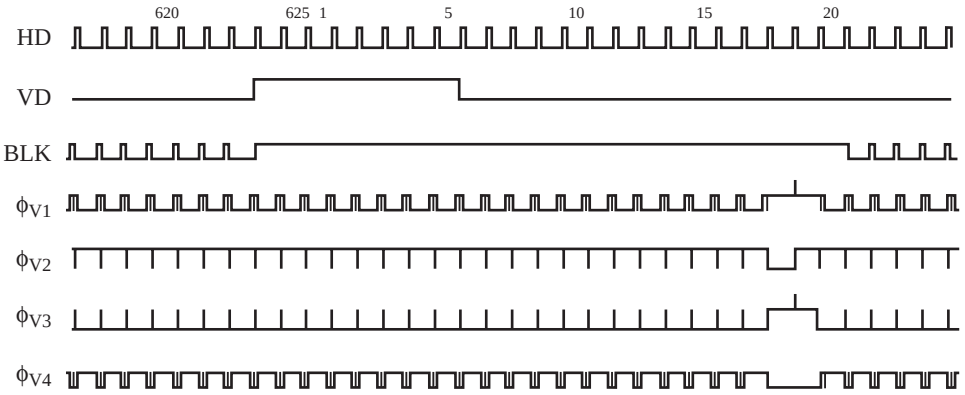


Color Filter Spectral Characteristics



■ Timing Diagram

< Field A >



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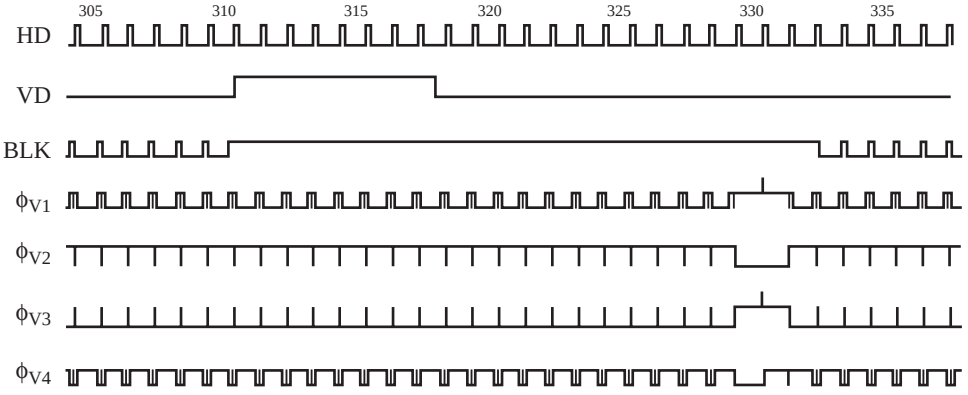
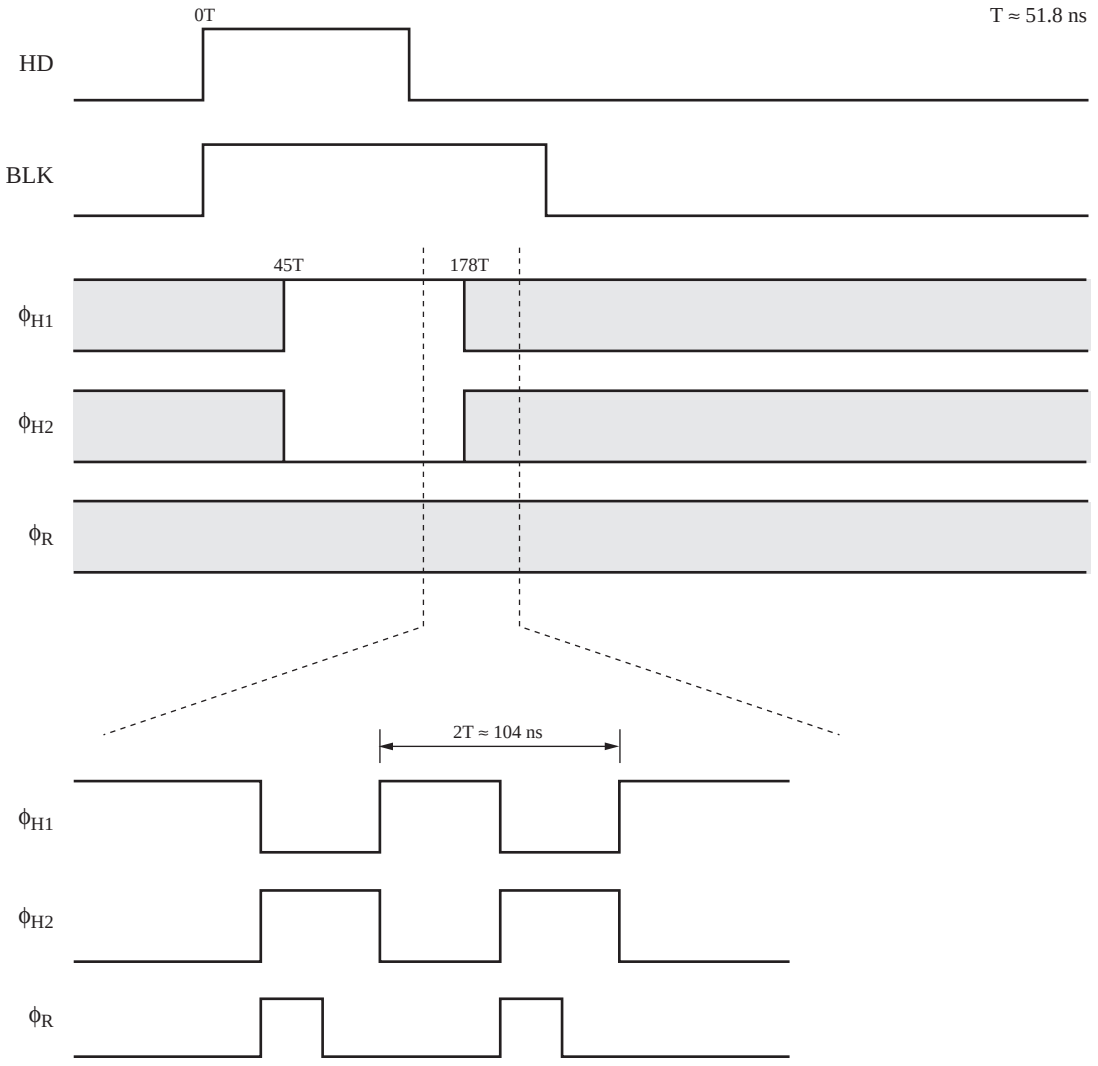


■ Timing Diagram (continued)



■ Package Dimensions (Unit：mm)

• WDIP016-P-0500C