MN37241FT

4.5mm (type-1/4) 480k pixels CCD Area Image Sensor

■ Overview

The MN37241FT is a 4.5 mm (type-1/4) interline transfer CCD (IT-CCD) solid state image sensor device with a total of 473,820 pixels. It provides optimum pixels for use in video cameras and security cameras, providing high sensitivity, low noise, broad dynamic range and low smear.

Part Number	Size	System	Color or B/W
MN37241FT	4.5mm(type-1/4)	PAL	Color

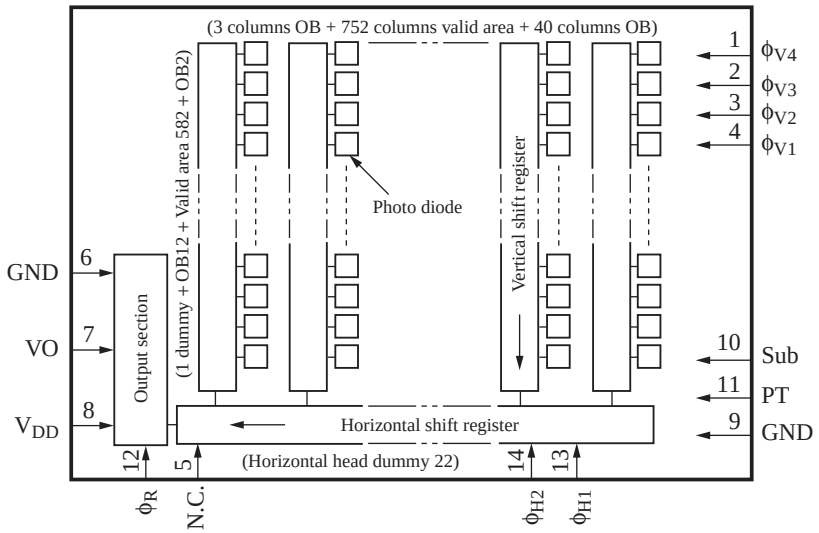
■ Features

- Total number of pixels: 795 (horizontal) × 596 (vertical)
- High sensitivity
- Low noise
- Non-adjusting (non-adjusting V_{Sub} reset voltage)
- Small size enables design of compact equipment

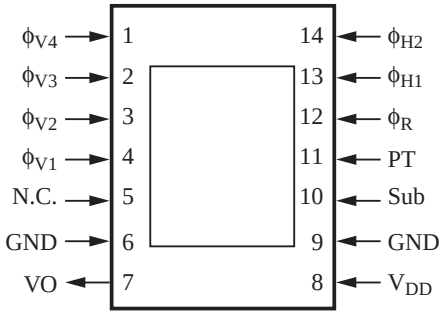
■ Applications

- Camera for multimedia use, Compact lightweight camcorders, Cameras for surveillance, measurement, and medical use

■ Block Diagram



■ Pin Assignments



(Top View)

■ Pin Descriptions

Pin No.	Symbol	Descriptions	Pin No.	Symbol	Descriptions
1	ϕ_{V4}	Vertical shift register clock pulse 4	6	GND	GND
			7	VO	Video output
2	ϕ_{V3}	Vertical shift register clock pulse 3	8	V_{DD}	Power supply
			9	GND	GND
3	ϕ_{V2}	Vertical shift register clock pulse 2	10	Sub	Substrate
			11	PT	P-well for protection circuit
4	ϕ_{V1}	Vertical shift register clock pulse 1	12	ϕ_R	Reset pulse (RG)
			13	ϕ_{H1}	Horizontal register clock pulse 1
5	N.C.	N.C.	14	ϕ_{H2}	Horizontal register clock pulse 2

■ Absolute Maximum Ratings and Operating Conditions

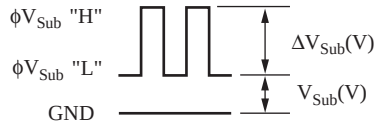
Parameter		Symbol	Rating		Operating condition			Unit
			min	max	min	typ	max	
Power supply voltage		V_{DD}	– 0.2	18.0	14.5	15.0	15.5	V
Protection P-well voltage		V_{PT} *2	– 10.0	0.2	– 7.8	– 7.5	– 7.2	V
GND		GND	Reference voltage		—	0	—	V
Reset	H-L	$V_{\phi R(H-L)}$	—	18.0	3.0	3.3	5.5	V
pulse voltage	Bias	$V_{\phi R(Bias)}$	Supplied internally					V
Horizontal register		$V_{\phi H1(H)}$	—	18.0	3.0	3.3	5.5	V
clock pulse voltage 1		$V_{\phi H1(L)}$	– 0.2	—	– 0.05	0	0.05	
Horizontal register		$V_{\phi H2(H)}$	—	18.0	3.0	3.3	5.5	V
clock pulse voltage 2		$V_{\phi H2(L)}$	– 0.2	—	– 0.05	0	0.05	
Vertical shift register		$V_{\phi V1(H)}$ *2	—	18.0	14.5	15.0	15.5	V
clock pulse voltage 1		$V_{\phi V1(M)}$ *2	—	—	– 0.2	0	0.2	
		$V_{\phi V1(L)}$ *2	– 9.0	—	– 8.3	– 8.0	– 7.7	
Vertical shift register		$V_{\phi V2(M)}$ *2	—	15.0	– 0.2	0	0.2	V
clock pulse voltage 2		$V_{\phi V2(L)}$ *2	– 9.0	—	– 8.3	– 8.0	– 7.7	
Vertical shift register		$V_{\phi V3(H)}$ *2	—	18.0	14.5	15.0	15.5	V
clock pulse voltage 3		$V_{\phi V3(M)}$ *2	—	—	– 0.2	0	0.2	
		$V_{\phi V3(L)}$ *2	– 9.0	—	– 8.3	– 8.0	– 7.7	
Vertical shift register		$V_{\phi V4(M)}$ *2	—	15.0	– 0.2	0	0.2	V
clock pulse voltage 4		$V_{\phi V4(L)}$ *2	– 9.0	—	– 8.3	– 8.0	– 7.7	
Substrate voltage		V_{Sub} *1	Supplied internally					V
		ΔV_{Sub} *3	– 0.2	35.0	21.7	22.5	23.3	
Operating temperature		T_{opr}	– 10	70	—	25	—	°C
Storage temperature		T_{stg}	– 30	80	—	—	—	°C

Note) 1. Standard light input defines

Standard light input is the one when the exposure is done at a lens aperture of F8, using a light source of 2856 K and 1050 nt, and placing a color temperature conversion filter LB-40 (HOYA) and an IR cutting filter CAW-500 (t = 2.5 mm) in the light path.

2. *1: V_{Sub} internal settings guarantee blooming at 400 times light input of the standard light input.
3. *2: V_{PT} is set so that the following conditions are set for VL of the vertical shift clock.

   $V_{PT} \leqq VL$
4. *3: V_{Sub} when using electronic shutter function

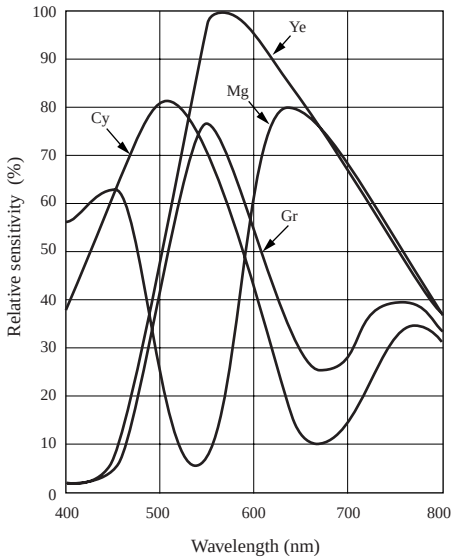


■ Optical Characteristics

Part Number	Color or B/W	Effective pixels H	Effective pixels V	S/N typ (dB)	Saturation output typ (mV)	Sensitivity F8 typ (mV)	Vertical smear Sm typ(%)	Image lag typ (%)	Horizontal resolution typ (TV-lines)	Vertical resolution typ (TV-lines)
MN37241FT	Color	752	582	42	500	200	0.01	—	480	420

■ Graphs of Characteristics

CCD On-Chip Filter Spectral Responsive Characteristics



■ Package Dimensions (Unit : mm)

• WDIP014-P-0400F