

MN37140FT

4.5 mm (type-1/4) 410k pixels CCD Area Image Sensor

Overview

The MN37140FT is a 4.5 mm (type-1/4) interline transfer CCD (IT-CCD) solid state image sensor device with a total of 411,988 pixels. It provides optimum pixels for use in video cameras and security cameras, providing high sensitivity, low noise, broad dynamic range and low smear.

Part Number	Size	System	Color or B/W
MN37140FT	4.5mm(type-1/4)	NTSC	Color

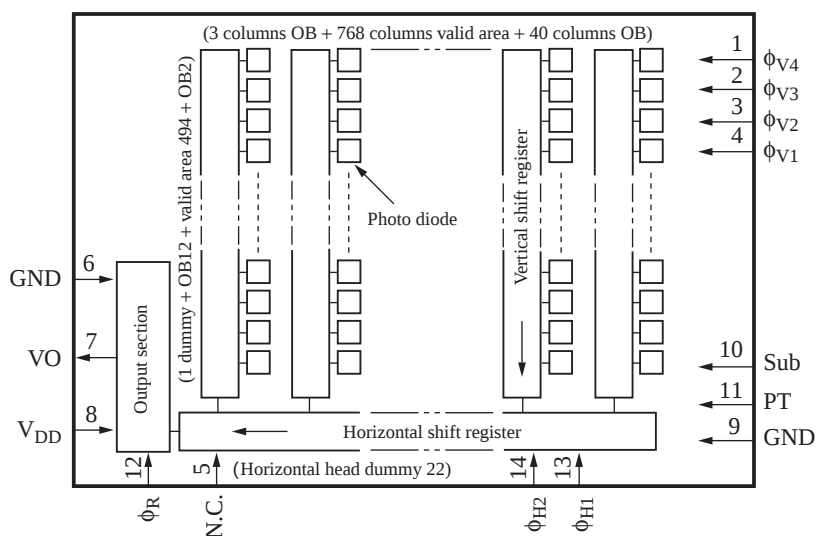
Features

- Total number of pixels : 811(horizontal) × 508(vertical)
- High sensitivity
- Low noise
- Non-adjusting (non-adjusting V_{Sub} reset voltage)
- Small size enables design of compact equipment

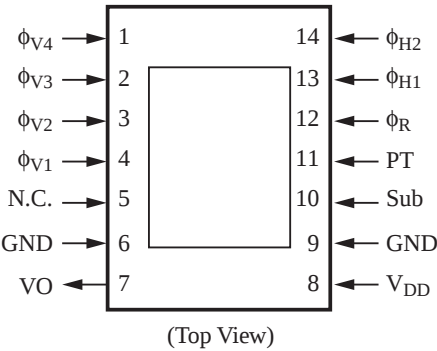
Applications

- Camera for multimedia use, Compact lightweight camcorders, Cameras for surveillance, measurement, and medical use

Block Diagram



■ Pin Assignments



■ Pin Descriptions

Pin No.	Symbol	Descriptions	Pin No.	Symbol	Descriptions
1	ϕ_{V4}	Vertical shift register clock pulse 4	6	GND	GND
			7	VO	Video output
2	ϕ_{V3}	Vertical shift register clock pulse 3	8	V_{DD}	Power supply
			9	GND	GND
3	ϕ_{V2}	Vertical shift register clock pulse 2	10	Sub	Substrate
			11	PT	P-well for protection circuit
4	ϕ_{V1}	Vertical shift register clock pulse 1	12	ϕ_R	Reset pulse (RG)
			13	ϕ_{H1}	Horizontal register clock pulse 1
5	N.C.	N.C.	14	ϕ_{H2}	Horizontal register clock pulse 2

Absolute Maximum Ratings and Operating Conditions

Parameter		Symbol	Rating		Operating condition			Unit
			min	max	min	typ	max	
Output drain voltage		V _{OD}	− 0.2	18.0	14.5	15.0	15.5	V
Protection P-well voltage		V _{PT} ^{*2}	− 10.0	0.2	− 7.3	− 7.0	− 6.7	V
GND		GND	Reference voltage		—	0	—	V
Reset	H-L	V _{φR(H-L)}	—	18.0	4.7	5.0	5.3	V
pulse voltage	Bias	V _{φR(Bias)}	Supplied internally					V
Horizontal register		V _{φH1(H)}	—	18.0	4.7	5.0	5.3	V
clock pulse voltage 1		V _{φH1(L)}	− 0.2	—	0	0	0	
Horizontal register		V _{φH2(H)}	—	18.0	4.7	5.0	5.3	V
clock pulse voltage 2		V _{φH2(L)}	− 0.2	—	0	0	0	
Vertical shift register		V _{φV1(H)} ^{*2}	—	18.0	14.5	15.0	15.5	V
clock pulse voltage 1		V _{φV1(M)} ^{*2}	—	—	− 0.2	0	0.2	
		V _{φV1(L)} ^{*2}	− 9.0	—	− 7.3	− 7.0	− 6.7	
Vertical shift register		V _{φV2(M)} ^{*2}	—	15.0	− 0.2	0	0.2	V
clock pulse voltage 2		V _{φV2(L)} ^{*2}	− 9.0	—	− 7.3	− 7.0	− 6.7	
Vertical shift register		V _{φV3(H)} ^{*2}	—	18.0	14.5	15.0	15.5	V
clock pulse voltage 3		V _{φV3(M)} ^{*2}	—	—	− 0.2	0	0.2	
		V _{φV3(L)} ^{*2}	− 9.0	—	− 7.3	− 7.0	− 6.7	
Vertical shift register		V _{φV4(M)} ^{*2}	—	15.0	− 0.2	0	0.2	V
clock pulse voltage 4		V _{φV4(L)} ^{*2}	− 9.0	—	− 7.3	− 7.0	− 6.7	
Substrate voltage		V _{Sub} ^{*1}	Supplied internally					V
		φV _{Sub} ^{*3}	− 0.2	45.0	24.5	25.0	25.5	
Operating temperature		T _{opr}	− 10	70	—	25	—	°C
Storage temperature		T _{stg}	− 30	80	—	—	—	°C

Note)1. Standard light input defines

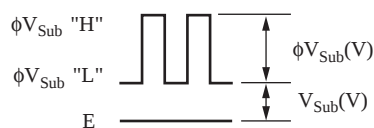
Standard light input is the one when the exposure is done at a lens aperture of F8, using a light source of 2856 K and 1050 nt, and placing a color temperature conversion filter LB-40 (HOYA) and an IR cutting filter CAW-500 (t = 2.5 mm) in the light path.

2. *1: V_{Sub} internal settings guarantee blooming at 400 times light input of the standard light input.

3. *2: V_{PT} is set so that the following conditions are set for VL of the vertical shift clock.

$$V_{PT} \leq VL$$

4. *3: V_{Sub} when using electronic shutter function

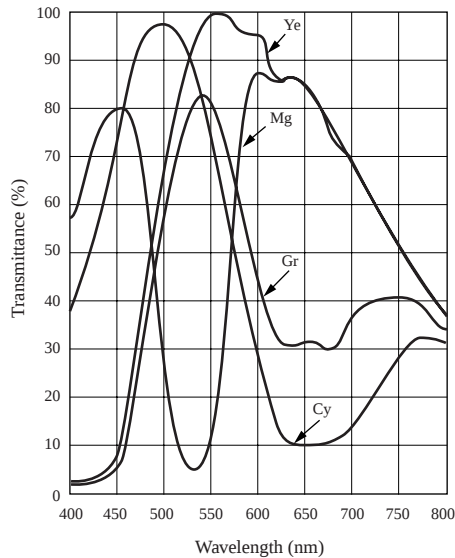


■ Optical Characteristics

Part Number	Color or B/W	Effective pixels		S/N typ (dB)	Saturation output typ (mV)	Sensitivity F8 typ (mV)	Vertical smear Sm typ(%)	Image lag typ (%)	Horizontal resolution typ (TV-lines)	Vertical resolution typ (TV-lines)
		H	V							
MN37140FT	Color	768	494	60	600	200	0.01	—	480	350

■ Graphs of Characteristics

CCD On-Chip Filter Spectral Responsive Characteristics



■ Package Dimensions (Unit : mm)

- WDIP014-P-0400F

