KAF-6302CE

3052 (H) x 2016 (V) Pixel

Full-Frame CCD Color Image Sensor

Performance Specification

Eastman Kodak Company

Image Sensor Solutions

Rochester, New York 14650-2010

Revision F

November 29, 1999

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FIGURES

APPENDICES

1.1   Features

- **6M Pixel Color Area CCD**

- **3052 (H) x 2016 (V) Photosensitive Pixels**

- **9? m (H) x 9? m (V) Pixels Size**

- **27.5mm (H) x 18.1mm (V) Photosensitive Area**

- **2-Phase Register Clocking**

- **Enhanced Responsivity**

- **Antiblooming Protection**

- **High Fill Factor (70%)**

- **High Output Sensitivity (10 µV/e⁻)**

- **Low Dark Current (< 10pA/cm² @ 25°C)**

1.2   Description

The KAF-6302CE is a high performance color area CCD (charge-coupled device) image sensor with 3052H x 2016V photoactive pixels designed for a wide range of color image sensing applications including digital imaging. Each pixel contains antiblooming protection by means of a lateral overflow drain thereby preventing image corruption during high light level conditions Each of the 9µm square pixels are selectively covered with red, green or blue filters for color separation. The photoactive pixels are surrounded by a border of buffer and light-shielded pixels as shown in Figure 1. Total chip size is 29.0mm x 19.1mm and is housed in a 26-pin, 0.88" wide DIL ceramic package with 0.1" pin spacing.
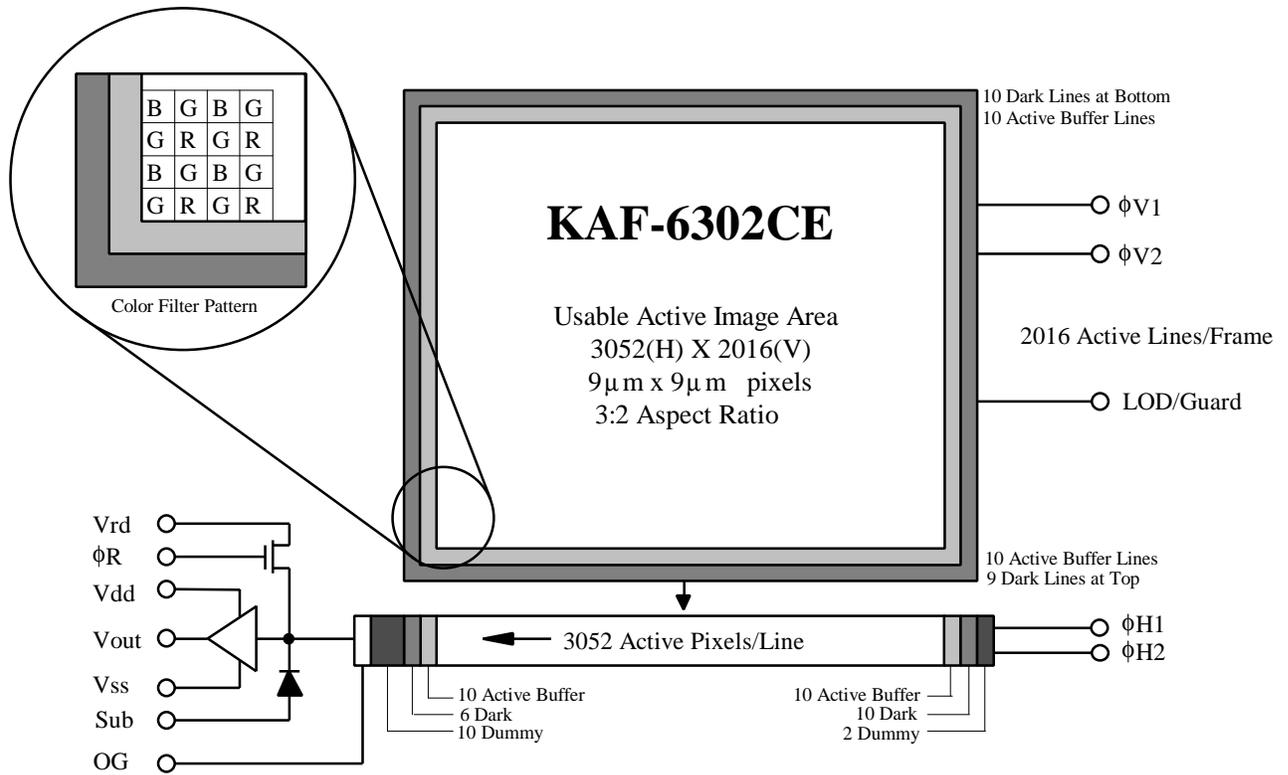

Figure 1 - Functional Block Diagram

1.3 Image Acquisition

An electronic representation of an image is formed when incident photons falling on the sensor plane create electron-hole pairs within the device. These photon induced electrons are collected locally by the formation of potential wells at each photogate or pixel site. The number of electrons collected is linearly dependent on light level and exposure time and non-linearly dependent on wavelength. When the pixel's capacity is reached, excess electrons are discharged into the lateral overflow drain to prevent crosstalk or 'blooming'. During the integration period, the $\phi V1$ and $\phi V2$ register clocks are held at a constant (low) level. See Figure 5. - Timing Diagrams.

1.4 Charge Transport

Referring again to Figure 5 - Timing Diagrams, the integrated charge from each photogate is transported to the output using a two step process. Each line (row) of charge is first transported from the vertical CCD's to a horizontal CCD register using the $\phi V1$ and $\phi V2$ register clocks. The horizontal CCD is presented a new line on the rising edge of $\phi V2$ while $\phi H1$ is held high. At the start of frame readout, the $\phi V2$ clock must be pulsed once prior to normal line clocking. The horizontal CCD's then transport each line, pixel by pixel, to the output structure by alternately clocking the $\phi H1$ and $\phi H2$ pins in a complementary fashion. On each falling edge of $\phi H2$ a new charge packet is dumped onto a floating diffusion and sensed by the output amplifier.

1.5 Output Structure

Charge presented to the floating diffusion (FD) is converted into a voltage and current amplified in order to drive off-chip loads. The resulting voltage change seen at the output is linearly related to the amount of charge placed on FD. Once the signal has been sampled by the system electronics, the reset gate (ϕR) is clocked to remove the signal and FD is reset to the potential applied by RD. More signal at the floating diffusion reduces the voltage seen at the output pin. In order to activate the output structure, an off-chip load must be added to the Vout pin of the device - see Figure 4.

1.6 Dark Reference Pixels

Surrounding the peripheral of the device is a border of light shielded pixels. This includes 6 leading and 10 trailing pixels on every line excluding dummy pixels. There are also 9 full dark lines at the start of every frame and 10 full dark lines at the end of each frame. Under normal circumstances, these pixels do not respond to light. However, dark reference pixels in close proximity to an active pixel, or the outer bounds of the chip (including the first two lines out), can scavenge signal depending on light intensity and wavelength.

1.7 Active Buffer Pixels

The first 10 pixels in from any dark reference regions are classified as active buffer pixels. These pixels are light sensitive but tend to have inconsistent spectral responsivities than the remainder of the array. Active buffer pixels are not tested for defects and uniformities.

1.8 Dummy Pixels

Within the horizontal shift register are 10 leading and 2 trailing additional shift phases which are not associated with a column of pixels within the vertical register. These pixels contain only horizontal shift register dark current signal and do not respond to light. A few leading dummy pixels may scavenge false signal depending on operating conditions.

2.1   Package Drawing
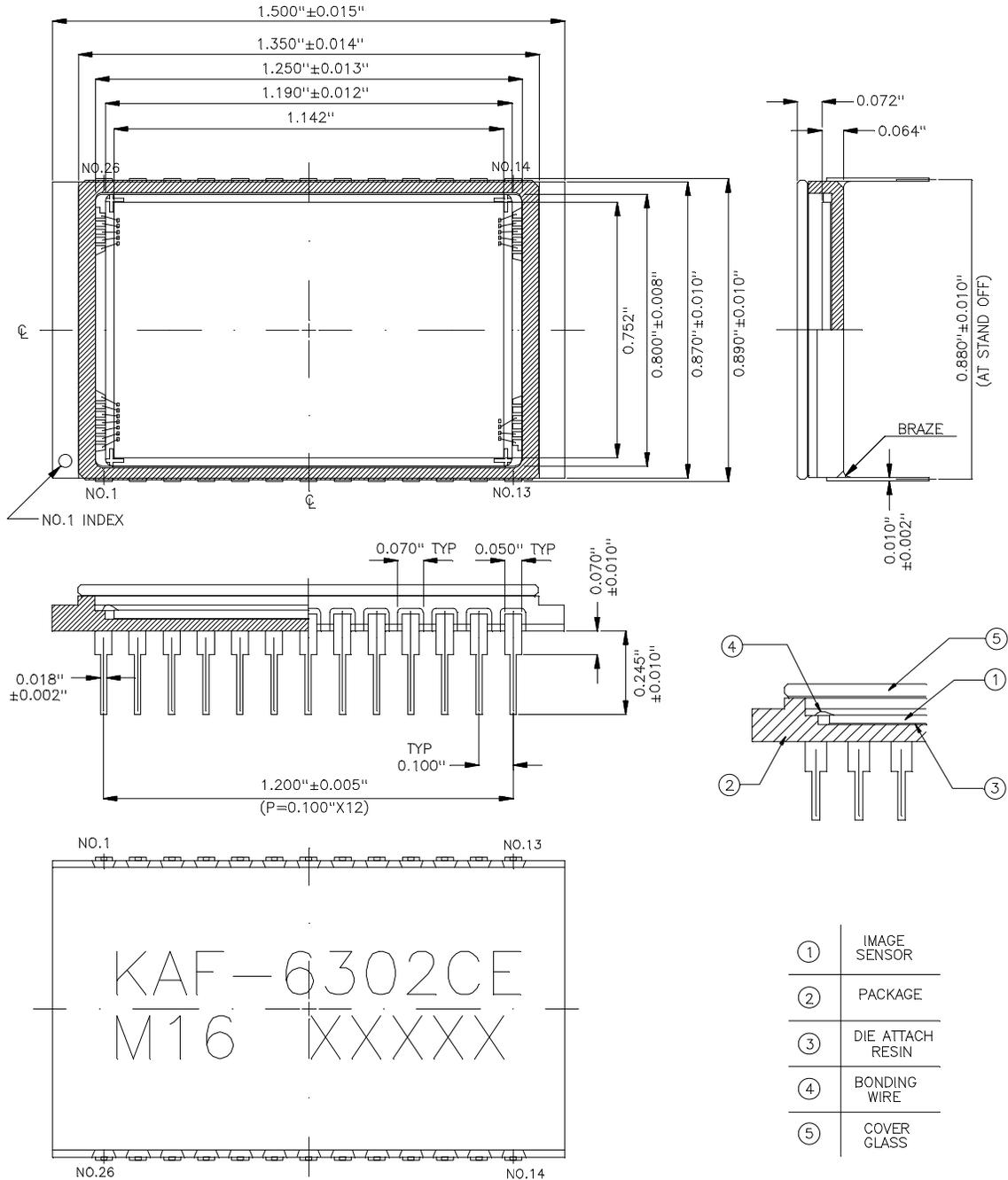
Figure 2 - Packaging Diagram

2.2 Pin Description

Pin	Symbol	Description	Pin	Symbol	Description
1, 6, 11, 12,13	Vsub	Substrate (Ground)	14, 15, 26	Vsub	Substrate (Ground)
2	Vout	Video Output	16, 17	ϕV1	Vertical CCD Clock - Phase 1
3	Vss	Amplifier Supply Return	18, 19	ϕV2	Vertical CCD Clock - Phase 2
4	Vrd	Reset Drain	20, 21	ϕV2	Vertical CCD Clock - Phase 2
5	ϕR	Reset Clock	22,23	ϕV1	Vertical CCD Clock - Phase 1
7	OG	Output Gate	24	LOD/Guard	Lateral Overflow Drain/Guard Ring
8	ϕH1	Horizontal CCD Clock - Phase 1	25	Vdd	Amplifier Supply
9	ϕH2	Horizontal CCD Clock - Phase 2			
10	N/C	No Connection (open pin)			
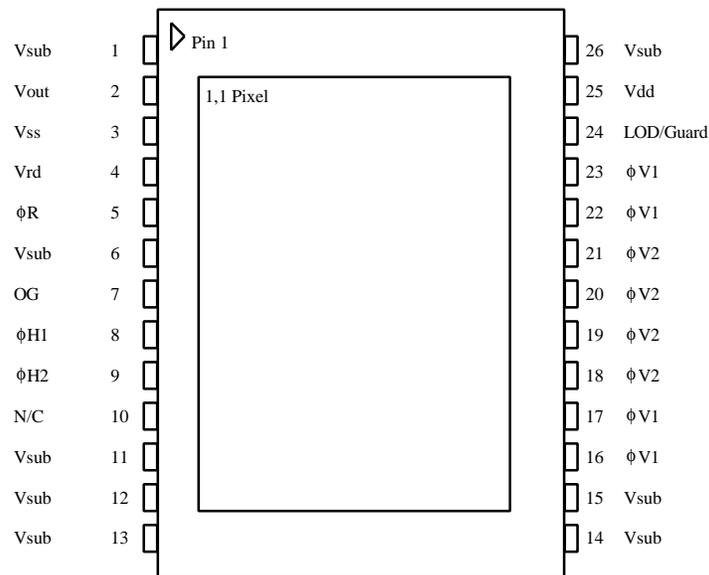
Figure 3 - Package Pin Designations

3.1 Absolute Maximum Ratings

Description	Symbol	Min.	Max.	Units	Notes
Diode Pin Voltages	Vdiode	0	16	V	1, 2
Gate Pin Voltages - Type 1	Vgate1	-10	10	V	1, 3
Gate Pin Voltages - Type 2	Vgate2	0	10	V	1,4
Inter-Gate Voltages	Vg-g		16	V	5
ϕV2-ϕH1 Voltages	V_{V-H}		17	V	6
ϕV1, ϕV2 - LOD Voltages	V_{V-L}		20	V	7
Output Bias Current	Iout		-10	mA	8
Output Load Capacitance	Cload		15	pF	8
Temperature	T	0	70	^{o}C	9
Humidity	RH	5	90	%	10

Notes:
1. Referenced to pin Vsub.
2. Includes pins: Vrd, Vdd, Vss, Vout, LOD/Guard.
3. Includes pins: ϕV1, ϕV2, ϕH1, ϕH2.
4. Includes pins with ESD protection: ϕR, OG.
5. Voltage difference between overlapping gates. Includes: ϕV1 to ϕV2, ϕH1 to ϕH2, ϕH2 to OG.
6. Voltage difference between overlapping gates. Includes: ϕV2 to ϕH1.
7. Voltage difference between ϕV1, ϕV2 gates and LOD/Guard diode.
8. Avoid shorting output pins to ground or any low impedance source during operation. Amplifier bandwidth increases at higher currents at the expense of reduced gain (sensitivity). Operation at these values will reduce MTTF.
9. Operating and storage temperature. Noise performance will degrade at higher temperatures. Long term storage at these temperatures will accelerate color filter degradation.
10. T=25°C. Excessive humidity will degrade MTTF.

CAUTION:	**This device contains limited protection against Electrostatic Discharge (ESD). Devices should be handled in accordance to strict ESD procedures for Class 1 devices.**

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3.2   DC Operating Conditions

Description	Symbol	Min.	Nom.	Max	Units	Max DC Current (mA)	Notes
Reset Drain	Vrd	11.3	11.5	11.7	V	0.01	
Output Amplifier Return	Vss	1.0	1.4	1.5	V	0.45	
Output Amplifier Supply	Vdd	14.5	15	15.5	V	Iout + Iss	
Substrate	Vsub		0		V	0.01	
Output Gate	OG	4.8	5.0	5.2	V	0.01	
Lateral Drain / Guard Ring	LOD/Guard	9.5	10.0	10.5	V	0.01	
Video Output Current	Iout		-5	-10	mA	-	1

Notes:

1.   An output load sink must be applied to Vout to activate output amplifier - see Figure below.
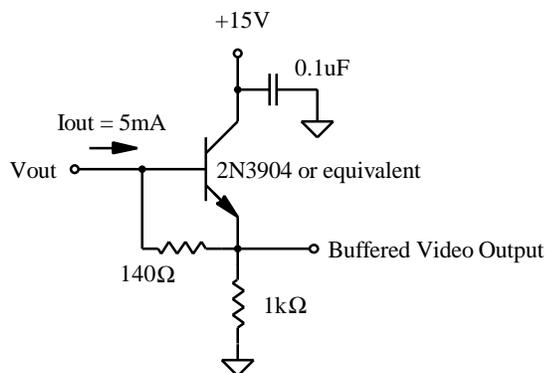
Component values may be revised based on operating conditions and other design considerations.

Figure 4 - Recommended Output Structure Load Diagram

3.3   AC Operating Conditions

Description	Symbol	Level	Min.	Nom.	Max.	Units	Est. Effective Capacitance	Notes
Vertical CCD Clock - Phase 1	$\phi V1$	Low	-8.7	-8.5	-8.3	V	221nF	1
		High	1.3	1.5	1.7	V	(total)	
Vertical CCD Clock - Phase 2	$\phi V2$	Low	-8.7	-8.5	-8.3	V	217nF	1
		High	1.3	1.5	1.7	V	(total)	
Horizontal CCD Clock - Phase 1	$\phi H1$	Low	-2.7	-2.5	-2.3	V	307pF	1
		High	7.3	7.5	7.7	V		
Horizontal CCD Clock - Phase 2	$\phi H2$	Low	-2.7	-2.5	-2.3	V	171pF	1
		High	7.3	7.5	7.7	V		
Reset Clock	ϕR	Low	3.3	3.5	3.7	V	9pF	1
		High	10.3	10.5	10.7	V		

Notes:
1. All pins draw less than 10µA DC current. Capacitance values relative to Vsub.

3.4   AC Timing Conditions

Description	Symbol	Min.	Nom.	Max.	Units	Notes
$\phi H1$, $\phi H2$ Clock Frequency	f_H		4	10	MHz	1, 2
$\phi V1$, $\phi V2$ Clock Frequency	f_V		50	167	kHz	1, 2
$\phi H1$, $\phi H2$ Rise / Fall Times		5		10	%	3
$\phi V1$, $\phi V2$ Rise / Fall Times		5		10	%	3
$\phi H1 - \phi H2$ Cross-over		30	50	70	%	4a
$\phi V1 - \phi V2$ Cross-over		-3	-1.5	0	V	4b
Pixel Period (1 Count)	t_e	143	250		ns	2
$\phi H1$, $\phi H2$ Setup Time	$t_{\phi HS}$	1	5		us	
ϕR Clock Pulse Width	$t_{\phi R}$	10	20		ns	5
$\phi V1$, $\phi V2$ Clock Pulse Width	$t_{\phi V}$	6	10		us	2
$\phi H2$ - Video Delay	t_{HV}		13		ns	
ϕR - Video Delay	t_{RV}		5		ns	
Readout Time	$t_{readout}$	950	1665		ms	7
Integration Time	t_{int}		Note 6			7
Line Time	t_{line}	462	810		us	8
Flush Time	t_{flush}	25	42		ms	

Notes:
1. 50% duty cycle values.
2. CTE will degrade above the nominal frequency.
3. Relative to the clock period (based on 10/90% of high/low levels)
4a. Relative to clock amplitude.
4b. Relative to ground.
5. ϕR should be clocked continuously.
6. Integration time is user specified.
7. Longer times will degrade noise performance.
8. First line out of each frame requires an additional $t_{\phi V}$ mount of time.

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Frame Timing

1 Frame = 2055 Lines

t_{int} $t_{readout}$

ϕV1

ϕV2 Line 1 2 3 2054 2055

ϕH1

ϕH2

Line 1 Timing Detail

$t_{line} + t_{\phi V}$

$t_{\phi V}$ $t_{\phi V}$

ϕV1

$t_{\phi V}$ $t_{\phi V}$

ϕV2 $t_{\phi HS}$ t_e

ϕH1 3100 Counts

ϕH2

ϕR

Lines 2-2055 Timing Detail

t_{line}

$t_{\phi V}$ $t_{\phi V}$

ϕV1

$t_{\phi V}$

ϕV2 $t_{\phi HS}$ t_e

ϕH1 3100 Counts

ϕH2

ϕR

Pixel Timing Detail

$t_{\phi R}$ t_e 1 Count

ϕR

ϕH1

ϕH2

t_{RV} t_{HV}

Vout Vodc

Vdark

Vsat Vsub

Line Content

ϕH1/ ϕH2 Count

1-10
11-16
17-26 27-3078 3079-3088
3089-3098
3099-3100

Dummy Pixels Photoactive Buffer Pixels

Dark Reference Pixels Photoactive Pixels *

* Lines 1-9 and 2046-2055 are full lines of dark reference pixels
  Lines 10-19 and 2036-2045 are full lines of photoactive buffer pixels

Power-up Flush Cycle

t_{flush} t_{int} $t_{readout}$

ϕV1

2055 Counts (Min)

ϕV2

ϕH1

3100 Counts (Min)

ϕH2

Figure 5 - Timing Diagrams

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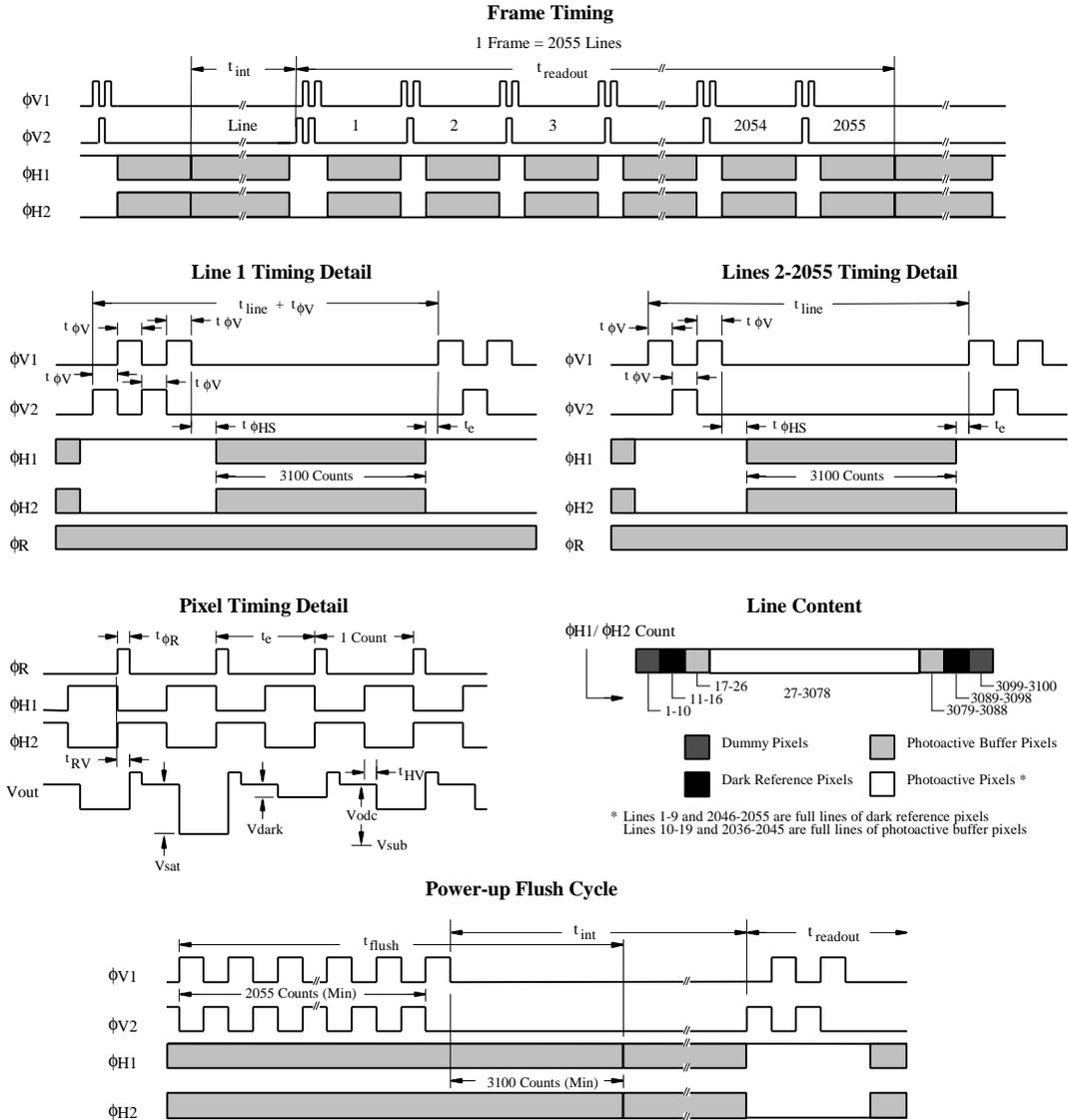
4.1   Performance Specifications

All values measured at 25°C, 4MHz data rates, tint = 250msec, treadout = 1665msec, nominal operating conditions and using the recommended output load circuits unless specified otherwise. These parameters exclude defective pixels.

Description	Symbol	Min.	Typ.	Max.	Units	Notes	Sampling
Saturation Signal	Vsat	500	550		mV	1a	die
Linear Saturation Signal	LVsat	450	500		mV	1a, 1b	die
Red Quantum Efficiency (λ=630nm)	Rr	11	13	15	%		
Green Quantum Efficiency (λ=540nm)	Rg	14	17	20	%		lot
Blue Quantum Efficiency (λ=440nm)	Rb	6	8	10	%		
High Level Photoresponse Non-Linearity	PRNL			1	%	2a	die
Low Level Photoresponse Non-Linearity	LLIN YINT	-3.0	-0.5	+3.0	mV	2b	die
Photoresponse Non-Uniformity	PRNU		12	15	%	3	die
Dark Signal	Vdark		0.5	2.0	mV	4	die
Dark Signal Non-Uniformity	DSNU		0.4	1.0	mV p-p	5	die
Dark Signal Doubling Temperature		5.0	6.3	7.0	°C		design
Read Noise	N		15		e⁻ rms	6	design
Linear Dynamic Range	DR	69	72		dB	7	design
Red Hue Shift	R HUE		5	10	%	8	die
Blue Hue Shift	B HUE		4	10	%	8	die
Charge Transfer Efficiency	CTE	0.99995*	0.99998*			9	die
Antiblooming Margin	Xab	8	100			10	die
Output Amplifier DC Offset	Vodc	10.5	11.5	12.5	V	11	die
Output Amplifier Bandwidth	f_{-3dB}	64	80		Mhz	12	die
Output Video Feedthrough	V_{oft}	80	120	160	mV	13	die
Reset Feedthrough	V_R		230	500	mV	14	die

Notes:
1a.   Increasing output load currents to improve bandwidth will decrease these values.
1b.   Maximum signal level achieved while meeting PRNL specification.
2.   Worst case deviation between Vsat/2 and Vsat relative to a linear fit applied between Vsat/2 ± Vsat/8 signal levels (center ¼ of data).
3.   Difference between the maximum and minimum average signal levels of 128 x 128 blocks within the sensor on a per color basis as a % of average signal level.
4.   Average non-illuminated signal w.r.t. over clocked horizontal register signal.
5.   Absolute difference between the maximum and minimum average signal levels of 64 x 64 blocks within the sensor.
6.   rms deviation of a multi-sampled pixel measured in the dark including amplifier noise sources.
7.   20log(Vsat/N) - see Note 6 and note 1b.
8.   Gradual variations in hue (red w.r.t. green pixels and blue w.r.t. green pixels) in regions of interest (128 x 128 blocks) within the sensor.
9.   Measured per transfer at Vsat min.
10.   Number of times above the Vsat illumination level required to bloom the sensor (all columns of imager).
11.   Video level offset w.r.t. ground
12.   Last stage only. Assumes 10pF off-chip load.
13.   Amount of artificial signal due to φH2 coupling.
14.   Amplitude of feedthrough pulse in Vout due to φR coupling.

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4.2   Typical Performance Characteristics

KAF-6302CE (Clear Coverglass)
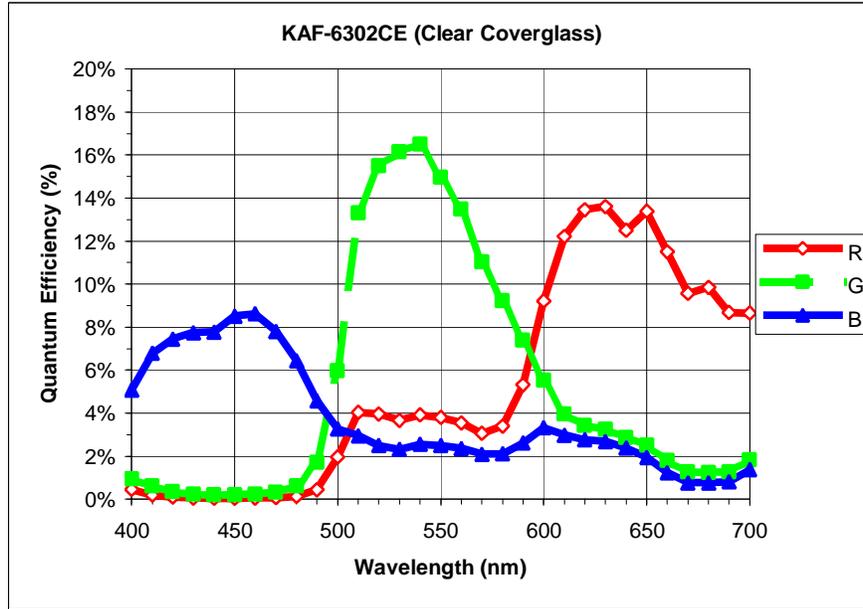
Figure 6 - Typical Quantum Efficiency Curves (Clear Cover Glass)

KAF-6302CE (IR Coverglass)
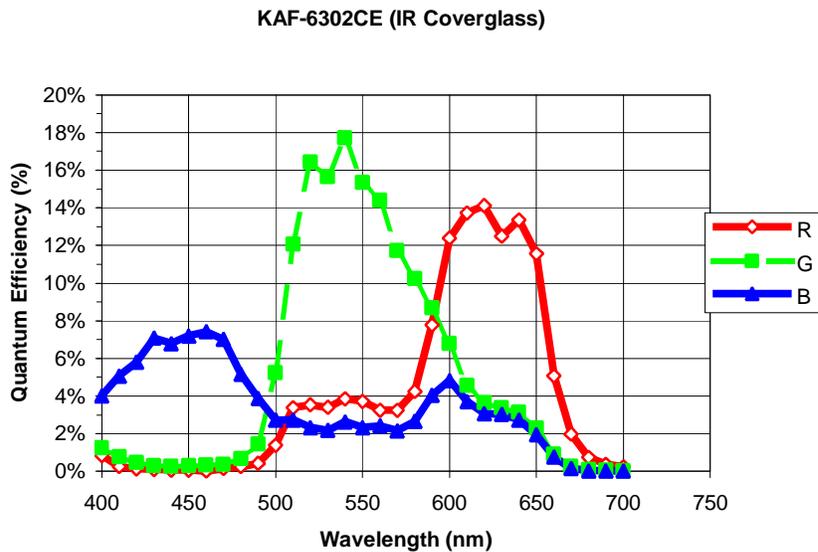
Figure 7 - Typical Quantum Efficiency Curves (IR Cover Glass)

4.3   Defect Classification

All defect tests performed at T=25°C, t_{int} = 250 msec and $t_{readout}$ = 1665 msec

Total Defects

Points	Clusters	Columns
Total	Total	Total
≤ 500	≤ 20	≤ 20

Point Defects   A pixel which deviates by more than 5mV above or below neighboring pixels under non-illuminated or low light level (<50mV) conditions
-- OR --
A pixel which deviates by more than 7% above or 11% below neighboring pixels under illuminated conditions.

Cluster Defect   A grouping of not more than 5 adjacent point defects.

Column Defect   A grouping of 6 or more point defects along a single column
-- OR --
A column which deviates by more than 0.5mV above or below neighboring columns under non-illuminated or low light level conditions
-- OR --
A column which deviates by more than 1.5% above or below neighboring columns under illuminated conditions

Column defects are separated by no less than 5 good columns in either direction

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5.1   Quality Assurance and Reliability

5.1.1   Quality Strategy: All devices will conform to the specifications stated in this document. This is accomplished through a combination of statistical process control and inspection at key points of the production process.

5.1.2   Replacement: All devices are warranted against failure in accordance with the terms of Terms of Sale.

5.1.3   Cleanliness: Devices are shipped free of contamination, scratches, etc. that would cause a visible defect.

5.1.4   ESD Precautions: Devices are shipped in a static-safe container and should only be handled at static-safe work stations.

5.1.5   Reliability: Information concerning the quality assurance and reliability testing procedures and results are available from the Microelectronics Technology Division and can be supplied upon request.

5.1.6   Test Data Retention: Devices have an identifying number of traceable to a test data file. Test data is kept for a period of 2 years after date of shipment.

5.2   Ordering Information

See Appendix 1 for available part numbers

Address all inquiries and purchase orders to:

Image Sensor Solutions
Eastman Kodak Company
Rochester, New York 14650-2010
Phone: (716) 722-4385
Fax: (716) 477-4947
E-mail: ccd@kodak.com

Kodak reserves the right to change any information contained herein without notice. All information furnished by Kodak is believed to be accurate.

Eastman Kodak Company – Image Sensor Solutions - Rochester, NY 14650-2010
Phone (716) 722-4385   Fax (716) 477-4947
Web: www.kodak.com/go/ccd   E-mail: ccd@kodak.com

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Appendix

Appendix 1 - Part Number Availability

Note: This appendix may be updated independently of the performance specification.
Contact Eastman Kodak for the latest revision

Device Name	Available Part Numbers	Features
KAF-6302CE	2H4754	3052(H) x 2016(V) Full-Frame Color CCD Image Sensor