KAF- 4202 Series

2032 (H) x 2044 (V) Pixel

Full-Frame CCD Image Sensor

Performance Specification

Eastman Kodak Company

Image Sensor Solutions

Rochester, New York 14650-2010

Revision 1

June 29, 2000

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FIGURES

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1.1 Features

- **4M Pixel Area CCD**
- **2032H x 2044V (9 µm) Pixels**
- **18.29 mm H x 18.40 mm V Photosensitive Area**
- **2-Phase Register Clocking**
- **Fill Factor**
- **Low Dark Current (<10pA/cm^2 @ 25°C)**

1.2 Description

The KAF-4202 is a high performance monochrome area CCD (charge-coupled device) image sensor with 2032 H x 2044V photo active pixels designed for a wide range of image sensing applications in the 0.4 nm to 1.0 nm wavelength band. Typical applications include military, scientific, and industrial imaging. A 74dB dynamic range is possible operating at room temperature.

The sensor is built with a true two-phase CCD technology. This technology simplifies the support circuits that drive the sensor and reduces the dark current without compromising charge capacity. The sensor is housed in a 26-pin, 1.36” wide DIL ceramic package with 0.1” pin spacing.

The sensor consists of 2048 parallel (vertical) CCD shift registers each 2048 elements long. These registers act as both the photosensitive elements and as the transport circuits that allow the image to be sequentially read out of the sensor. The elements of these registers are arranged into a 2032 x 2044 photosensitive array surrounded by a light shielded dark reference of 16 columns and 4 rows. The parallel (vertical) CCD registers transfer the image one line at a time into a single 2060 element (horizontal) CCD shift register. The horizontal register transfers the charge to a single output amplifier. The output amplifier is a two-stage source follower that converts the photo-generated charge to a voltage for each pixel.

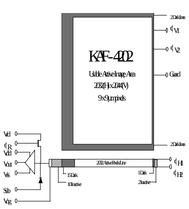

Figure 1 - Functional Block Diagram

1.3 Image Acquisition

An electronic representation of an image is formed when incident photons falling on the sensor plane create electron-hole pairs within the sensor. These photon induced electrons are collected locally by the formation of potential wells at each photogate or pixel site. The number of electrons collected is linearly dependent on light level and exposure time and non-linearly dependent on wavelength. When the pixel's capacity is reached, excess electrons will leak into the adjacent pixels within the same column. This is termed blooming. During the integration period, the ϕV1 and ϕV2 register clocks are held at a constant (low) level.
See Figure 5. - Timing Diagrams.

1.4 Charge Transport

Referring again to Figure 5 - Timing Diagrams, the integrated charge from each photogate is transported to the output using a two step process. Each line (row) of charge is first transported from the vertical CCD's to the horizontal CCD register using the ϕV1 and ϕV2 register clocks. The horizontal CCD is presented a new line on the falling edge of ϕV2 while ϕH1 is held high. The horizontal CCD's then transport each line, pixel by pixel, to the output structure by alternately clocking the ϕH1 and ϕH2 pins in a complementary fashion. On each falling edge of ϕH2 a new charge packet is transferred onto a floating diffusion and sensed by the output amplifier

1.5 Output Structure

Charge presented to the floating diffusion (FD) is converted into a voltage and current amplified in order to drive off-chip loads. The resulting voltage change seen at the output is linearly related to the amount of charge placed on FD. Once the signal has been sampled by the system electronics, the reset gate (ϕR) is clocked to remove the signal and FD is reset to the potential applied by Vrd. More signal at the floating diffusion reduces the voltage seen at the output pin. In order to activate the output structure, an off-chip load must be added to the Vout pin of the device - see Figure 4.

1.6 Dark Reference Pixels

Surrounding the peripheral of the device is a border of light shielded pixels. This includes 15 leading and 1 trailing pixels on every line excluding dummy pixels. There are also 2 full dark lines at the start of every frame and 2 full dark lines at the end of each frame. Under normal circumstances, these pixels do not respond to light. However, dark reference pixels in close proximity to an active pixel, or the outer bounds of the chip (including the dark shielded lines), can scavenge signal depending on light intensity and wavelength and therefore will not represent the true dark signal.

1.7 Dummy Pixels

Within the horizontal shift register are 10 leading and 2 trailing additional shift phases which are not associated with a column of pixels from the vertical register. These pixels contain only horizontal shift register dark current signal and do not respond to light. A few leading dummy pixels may scavenge false signal depending on operating conditions.

2.1 Package Drawing

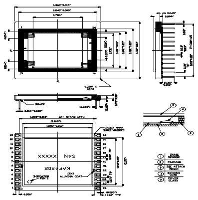

Figure 2 - Package Drawing

2.2 Pin Description

Pin	Symbol	Description	Pin	Symbol	Description
1, 2, 25, 26	φV2	Vertical CCD Clock - Phase 2	10	Vrd	Reset Drain
3, 4, 23, 24	φV1	Vertical CCD Clock - Phase 1	11	φR	Reset Clock
5	Vguard	Guard Ring	12	Vss	Amplifier Supply Return
6, 18, 22	Vsub	Substrate (Ground)	13, 14, 15, 19, 20, 21	N/C	No connection (open pin)
7	Vog	Output Gate	16	φH1	Horizontal CCD Clock - Phase 1
8	Vout	Video Output	17	φH2	Horizontal CCD Clock - Phase 2
9	Vdd	Amplifier Supply			

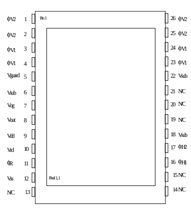

Figure 3 - Package Pin Designations

3.1 Absolute Maximum Ratings

Description	Symbol	Min.	Max.	Units	Notes
Diode Pin Voltages	Vdiode	0	20	V	1, 2
Gate Pin Voltages - Type 1	Vgate1	-16	16	V	1,3
Gate Pin Voltages - Type 2	Vgate2	0	16	V	1, 4
Inter-Gate Voltages	Vg-g		16	V	5
Output Bias Current	Iout		-10	mA	6
Output Load Capacitance	Cload		15	pF	6
Storage Temperature	Ts	0	80	^{o}C	7, 8
Operating Temperature	Top	-70	70	^{o}C	8, 9

Notes:
1. Referenced to pin Vsub.
2. Includes pins: Vrd, Vdd, Vss, Vout, Vguard.
3. Includes pins: ϕV1, ϕV2, ϕH1, ϕH2.
4. Includes pins: ϕR, Vog.
5. Voltage difference between overlapping gates. Includes: ϕV1 to ϕV2, ϕH1 to ϕH2, ϕV2 to ϕH1, ϕH2 to Vog.
6. Avoid shorting output pins to ground or any low impedance source during operation.
7. This refers to normal storage of a non-operating component. The sensor can be stored at lower temperatures in a non-condensing environment.
8. Sensors with temporary cover glass are not hermetically sealed and their life time will be adversely affected in a warm, humid environment. These sensors should be operated in evacuated or back-filled dry environments.
9. The dynamic range is reduced at higher temperatures due to increases in the dark signal level.

CAUTION: This device contains limited protection against Electrostatic Discharge (ESD). Devices should be handled in accordance to strict ESD procedures for Class 1 devices.

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3.2 DC Operating Conditions

Description	Symbol	Min.	Nom.	Max.	Units	Max DC Current (mA)	Notes
Reset Drain	Vrd	10.75	11	12	V	0.01	
Output Amplifier Return	Vss	1.5	2.0	2.5	V	0.45	
Output Amplifier Supply	Vdd	14.5	15	15.5	V	Iout	
Substrate	Vsub	0	0	0	V	0.01	
Output Gate	Vog	3.75	4.0	5.0	V	0.01	
Guard Ring	Vguard	8.0	10.0	12.0	V	0.01	
Video Output Current	Iout		-5	-10	mA	-	1

Notes:
1. An output load sink must be applied to Vout to activate output amplifier - see Figure 4 below.

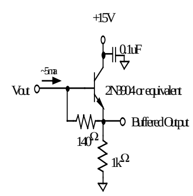


Figure 4 - Recommended Output Structure Load Diagram

3.3 AC Operating Conditions

Description	Symbol	Level	Min.	Nom.	Max.	Units	Effective Capacitance	Notes
Vertical CCD Clock - Phase 1	ϕV1	Low High	-9.0 0.5	-8.0 1.0	-7.5 1.5	V V	200nF (all ϕV1 pins)	
Vertical CCD Clock - Phase 2	ϕV2	Low High	-9.0 0.5	-8.0 1.0	-7.5 1.5	V V	200nF (all ϕV2 pins)	
Horizontal CCD Clock - Phase 1	ϕH1	Low High	-6.0 4.0	-4.0 6.0	-3.5 6.5	V V	150pF	
Horizontal CCD Clock - Phase 2	ϕH2	Low High	-6.0 4.0	-4.0 6.0	-3.5 6.5	V V	150pF	
Reset Clock	ϕR	Low High	-5.0 3.5	-3.0 4.0	-2.0 5.0	V V	10pF	

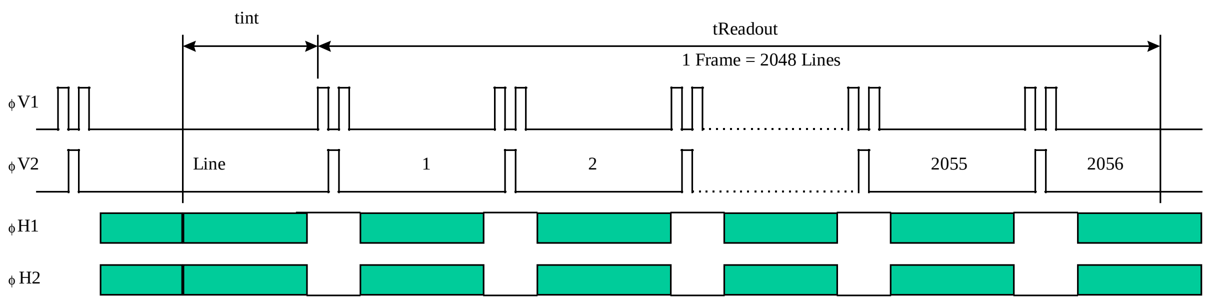
Notes:
1. All pins draw less than 10uA DC current.
2. Capacitance values relative to VSUB.

3.4 AC Timing Conditions

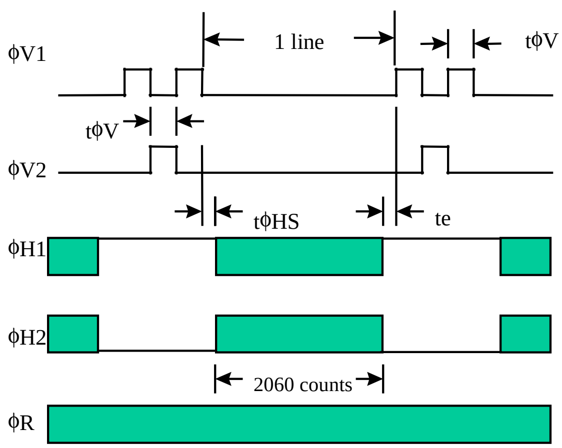
Description	Symbol	Min.	Nom.	Max.	Units	Notes
ϕH1, ϕH2 Clock Frequency	f_H		4	15	MHz	1, 2, 3
ϕV1, ϕV2 Clock Frequency	f_V		25	50	kHz	1, 2, 3
Pixel Period (1 Count)	t_e	67	250		ns	
ϕH1, ϕH2 Setup Time	$t_{\phi HS}$	0.5	1		us	
ϕV1, ϕV2 Clock Pulse Width	$t_{\phi V}$	10	20		us	2
Reset Clock Pulse Width	$t_{\phi R}$	10	20		ns	4
Readout Time	$t_{readout}$	531	1719		ms	5
Integration Time	t_{int}					6
Line Time	t_{line}	258.2	836		us	7

Notes:
1. 50% duty cycle values.
2. CTE may degrade above the nominal frequency.
3. Rise and fall times (10/90% levels) should be limited to 5-10% of clock period. Cross-over of register clocks should be between 40-60% of amplitude.
4. ϕR should be clocked continuously.
5. $t_{readout} = (2044 * t_{line})$
6. Integration time is user specified. Longer integration times will degrade noise performance.
7. $t_{line} = (3 * t_{\phi V}) + t_{\phi HS} + (2060 * t_e) + t_e$

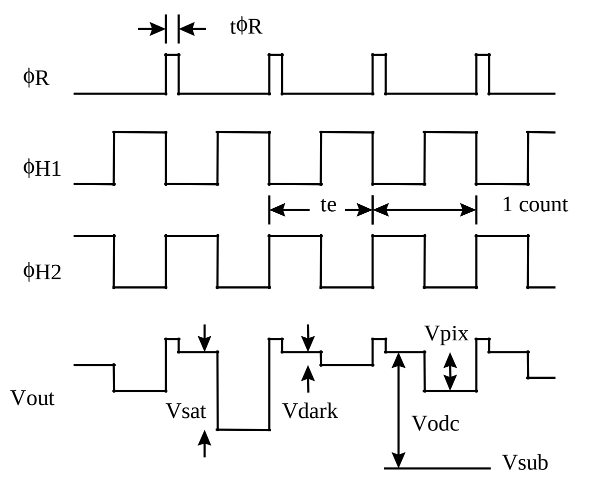
Frame Timing



Line Timing Detail



Pixel Timing Detail



Vsat	Saturated pixel video output signal
Vdark	Video output signal in no light situation, not zero due to Jdark
Vpix	Pixel video output signal level, more electrons =more negative*
Vodc	Video level offset with respect to vsub
Vsub	Analog Ground

* See Image Aquisition section (page 4)

Line Content

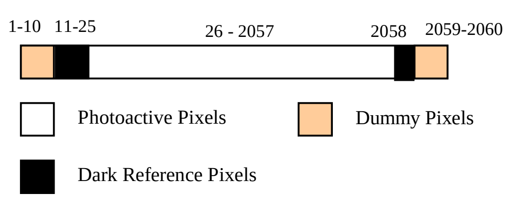


Figure 5 - Timing Diagrams

4.1 Performance Specifications

All values measured at 25°C, and nominal operating conditions. These parameters exclude defective pixels.

Description	Symbol	Min.	Nom.	Max.	Units	Notes
Saturation Signal Vertical CCD capacity Horizontal CCD capacity Output Node capacity	Nsat	85,000 170,000 19,0000	100,000 200,000 200,000	120,000 240,000 220,000	electrons / pixel	1
Red Quantum Efficiency (λ=650nm) Green Quantum Efficiency (λ=550nm) Blue Quantum Efficiency (λ=450nm)	Rr Rg Rb	28 28 9.8	35 35 12	41 41 14	% % %	
Photoresponse Non-Linearity	PRNL		1	2	%	2
Photoresponse Non-Uniformity	PRNU		1	3	%	3
Dark Signal	Jdark		15 3.5	50 10	electrons / pixel / sec pA/cm^2	4
Dark Signal Doubling Temperature		5	6.3	7.5	°C	
Dark Signal Non-Uniformity	DSNU		15	50	electrons / pixel / sec	5
Dynamic Range	DR	70	74		dB	6
Charge Transfer Efficiency	CTE	0.99997	0.99998			
Output Amplifier DC Offset	Vodc	10.5	11.5	12.5	V	7
Output Amplifier Bandwidth	f_{-3dB}		45		Mhz	8
Output Amplifier Sensitivity	Vout/Ne~	9	10	11	uV/e~	
Output Amplifier output Impedance	Zout	175	200	250	Ohms	
Noise Floor	ne~		15	20	electrons	9

Notes:

1. For pixel binning applications, electron capacity up to 330000 can be achieved with modified CCD inputs. Each sensor may have to be optimized individually for these applications. Some performance parameters may be compromised to achieve the largest signals.
2. Worst case deviation from straight line fit, between 1% and 90% of Vsat.
3. One Sigma deviation of a 128x128 sample when CCD illuminated uniformly.
4. Average of all pixels with no illumination at 25°C.
5. Average dark signal of any of 12 x 8 blocks within the sensor. (Each block is 128 x 128 pixels.)
6. 20log (Nsat / ne~) at nominal operating frequency and 25°C.
7. Video level offset with respect to ground.
8. Last output amplifier stage only. Assumes 10pF off-chip load.
9. Output noise at 25°C, nominal operating frequency, and tint = 0.

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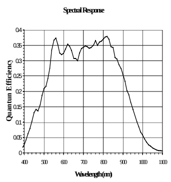
4.2 Typical Performance Characteristics



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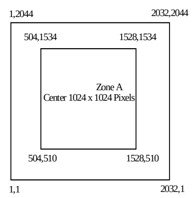
4.3 Defect Classification

Defect tests performed at T=25^{o}C

Class	Point Defects		Cluster Defects		Column Defects	
	Total	Zone A	Total	Zone A	Total	Zone A
C1	≤15	≤6	0	0	0	0
C2	≤30	≤15	≤12	≤6	≤6	0
C3	≤60	≤30	≤24	≤12	≤12	≤6



Point Defect	Dark:	A pixel which deviates by more than 6% from neighboring pixels when illuminated to 70% of saturation, OR
	Bright:	A Pixel with dark current > 10,000 e/pixel/sec at 25C.
Cluster Defect		A grouping of not more than 5 adjacent point defects

Column Defect A grouping of >5 contiguous point defects along a single column, OR
A column containing a pixel with dark current > 30,000e/pixel/sec, OR A column that does not meet the CTE specification for all exposures less than the specified Max sat. signal level and greater than 2 Ke, OR
A pixel which loses more than 250 e under 2Ke illumination.

Neighboring pixels	The surrounding 128 x 128 pixels or ±64 columns/rows.
Defect Separation	Column and cluster defects are separated by no less than two (2) pixels in any direction (excluding single pixel defects).
Defect Region Exclusion	Defect region excludes the outer two (2) rows and columns at each side/end of the sensor.

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5.1 Quality Assurance and Reliability

5.1.1 Quality Strategy: All devices will conform to the specifications stated in this document. This is accomplished through a combination of statistical process control and inspection at key points of the production process.

5.1.2 Replacement: All devices are warranted against failure in accordance with the terms of Terms of Sale.

5.1.3 Cleanliness: Devices are shipped free of contamination, scratches, etc. that would cause a visible defect.

5.1.4 ESD Precautions: Devices are shipped in a static-safe container and should only be handled at static-safe workstations.

5.1.5 Reliability: Information concerning the quality assurance and reliability testing procedures and results are available from the Image Sensor Solutions and can be supplied upon request.

5.1.6 Test Data Retention: Devices have an identifying number of traceable to a test data file. Test data is kept for a period of 2 years after date of shipment.

5.2 Ordering Information

See Appendix 1 for available part numbers

Address all inquiries and purchase orders to:

Microelectronic Technology Division
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Eastman Kodak reserves the right to change any information contained herein without notice.
All information furnished by Eastman Kodak is believed to be accurate.

WARNING: LIFE SUPPORT APPLICATIONS POLICY

Eastman Kodak image sensors are not authorized for and should not be used within Life Support Systems without the specific written consent of the Eastman Kodak Company. Product warranty is limited to replacement of defective components and does not cover injury or property or other consequential damages.

Appendix

Appendix 1 - Part Number Availability

Note: This appendix may be updated independently of the performance specification. Contact Eastman Kodak for the latest revision

Device Name	Available Part Numbers	Features
KAF-4202	2H4223	Monochrome, Clear Sealed Glass : Class 1
KAF-4202	2H4224	Monochrome, Clear Sealed Glass : Class 2
KAF-4202	2H4220	Monochrome, Clear Sealed Glass : Class 3
KAF-4202	2H4226	Monochrome, Clear Sealed Glass : Engineering Grade
KAF-4202	2H4227	Monochrome, Clear Sealed Glass : Mechanical Grade
KAF-4202	2H4229	Monochrome, Clear Taped Glass : Class 1
KAF-4202	2H4230	Monochrome, Clear Taped Glass : Class 2
KAF-4202	2H4221	Monochrome, Clear Taped Glass : Class 3
KAF-4202	2H4232	Monochrome, Clear Taped Glass : Engineering Grade
KAF-4202	2H4233	Monochrome, Clear Taped Glass : Mechanical Grade