KAI - 4000M

2048 (H) x 2048 (V) Pixel

Megapixel Interline CCD Image Sensor

Performance Specification

Eastman Kodak Company

Image Sensor Solutions

Rochester, New York 14650-2010

Revision 1

December 20, 1999

Eastman Kodak Company – Image Sensor Solutions - Rochester, NY 14650-2010
Phone (716) 722-4385 Fax (716) 477-4947
Web: www.kodak.com/go/ccd E-mail: ccd@kodak.com

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Eastman Kodak Company – Image Sensor Solutions - Rochester, NY 14650-2010
Phone (716) 722-4385 Fax (716) 477-4947
Web: www.kodak.com/go/ccd E-mail: ccd@kodak.com

1.1 Image Sensor Features

- **4.2 million pixels, 2048 (H) by 2048 (V)**
- **7.4 mm square pixels**
- **Progressive scan (noninterlaced)**
- **HCCD and output amplifier capable of 20 MHz operation**
- **Four video outputs, one at each corner of the sensor**
- **Each output has 28 light shielded columns**
- **Only 2 vertical CCD clocks and 2 horizontal CCD clocks**
- **15 Frames per second at full resolution using 20 MHz pixel rate**
- **30 Frames per second with 2 x 2 binning, 1024 x 1024 pixel resolution**
- **60 Frames per second with 4 x 4 binning, 512 x 512 pixel resolution**
- **15.2 mm x 15.2 mm imaging area**
- **Electronic shutter**
- **Low Dark Current**
- **Antiblooming protection**

1.2 Description

The KAI-4000M is a high performance interline charge-coupled device (CCD) designed for a wide range of medical imaging and machine vision applications. The device is built using an advanced two-phase, double-polysilicon, NMOS CCD technology. The p+npn- photodiodes eliminate image lag while providing antiblooming protection and electronic shutter capability. The 7.4 μm square pixels with microlenses provide high sensitivity and large dynamic range. The four outputs and several binning modes enable 15 to 60 frame per second (fps) video rate with this four megapixel progressive scan imager.

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1.3 Image Sensor Layout

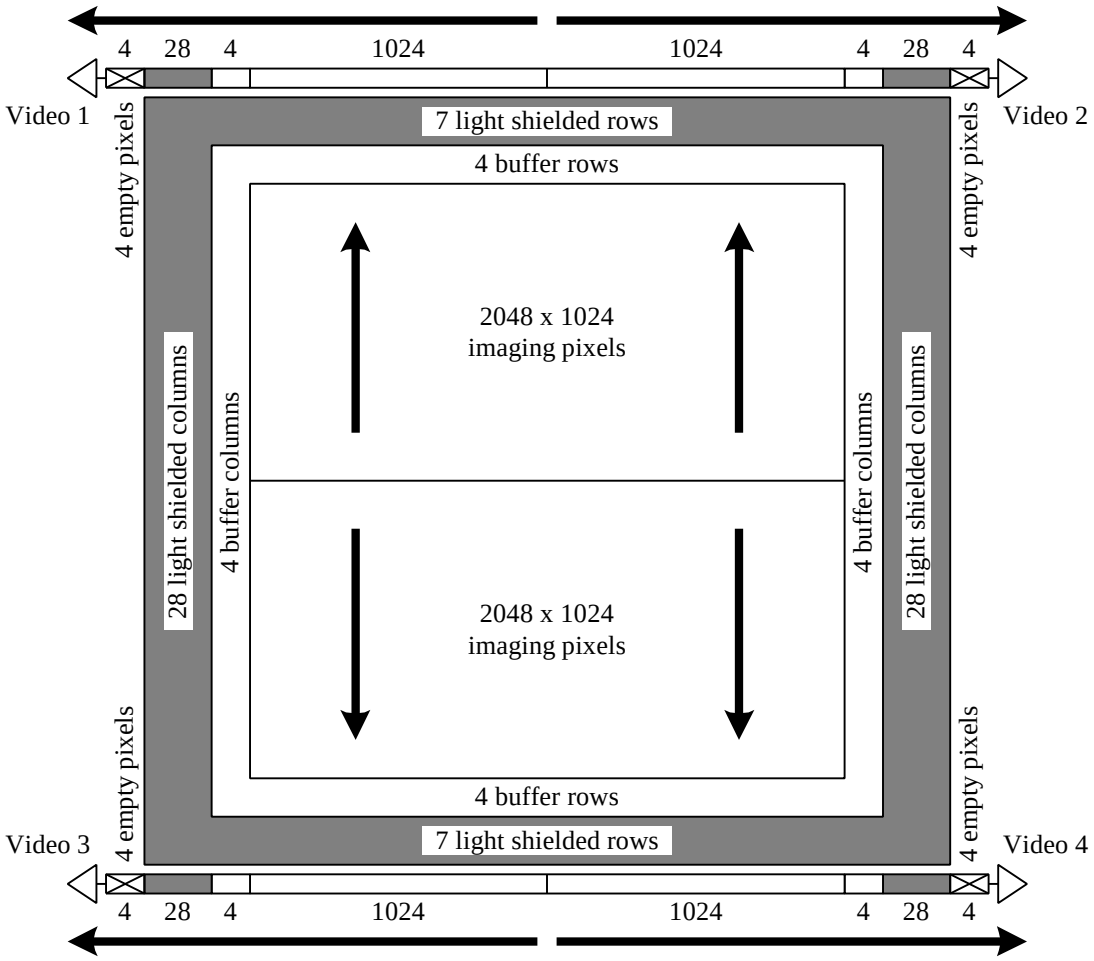

Figure 1 - Sensor Architecture

There are four video outputs, one at each corner of the image sensor. There are two horizontal shift registers, one at the top and one at the bottom of the image sensor. The top 1035 rows are transferred into the top horizontal shift register. The bottom 1035 rows are transferred into the bottom horizontal shift register. Each horizontal shift register is split into a left and right section. Each video output receives image data from a 1060 (H) by 1035 (V) region of the sensor. The total photoactive area is 2048 (H) by 2048 (V) pixels with a four pixel photoactive buffer zone around the perimeter of the sensor.

The first four pixels of each horizontal shift register are empty pixels that do not receive charge from a vertical shift register. The next 28 pixels receive charge from the 28 light shielded columns. The following 1028 pixels receive charge from photoactive columns. Only the center 26 of the 28 light shielded columns should be used as a dark reference. The first and last light shielded columns may be weakly responsive to light. Of the seven light shielded rows, only rows 5 and 6 can be used as a dark reference.

2.1 Package Drawing

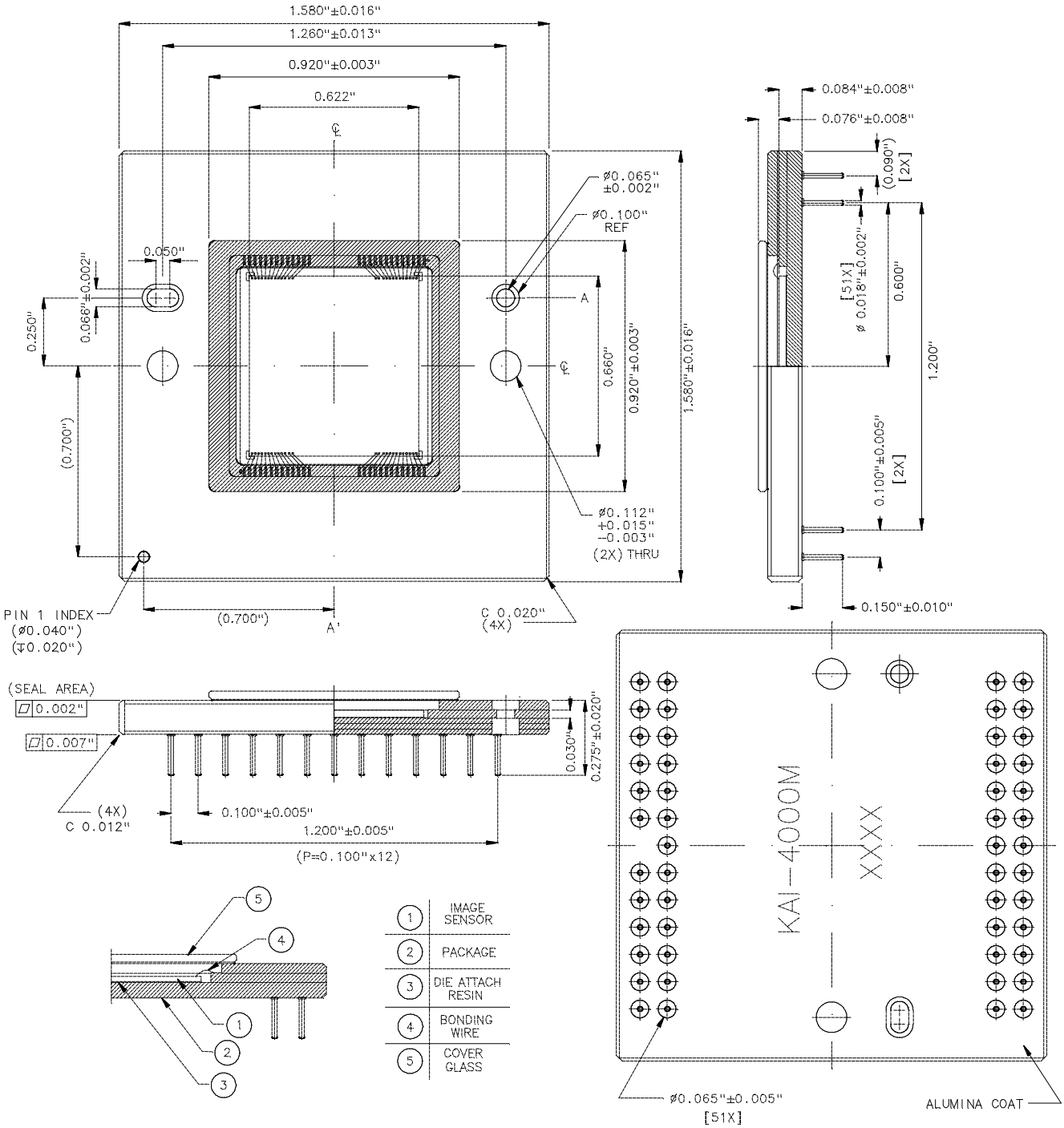

Figure 2 - Package Drawing

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2.2 Pin Description

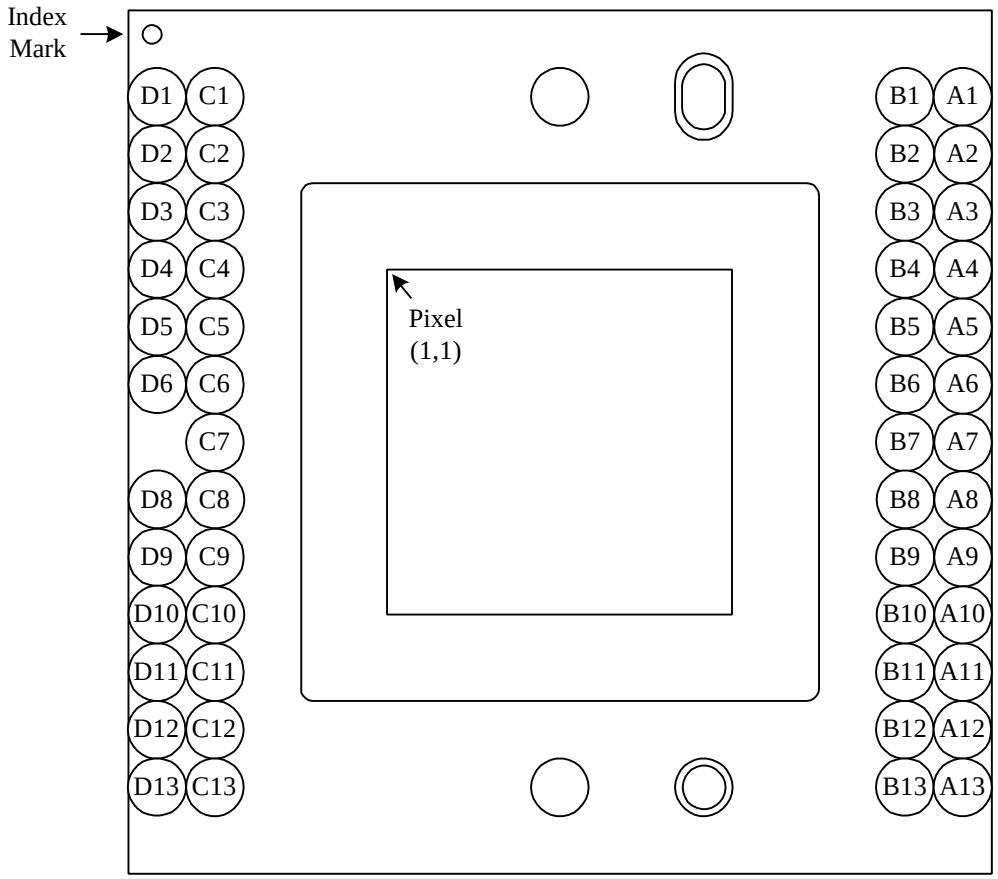

Figure 3 - Package Pin Designations - Top View

Pin	Label	Function	Notes
A1	ϕH2	Horizontal CCD phase 2 (top)	1, 3
A2	OG	Output Gate	
A3	RD	Reset Drain	
A4	VLG	Amplifier Load Gate	
A5	VDD	Output Amplifier Supply	
A6	ϕV1	Vertical CCD phase 1	
A7	ESD	ESD Protection	
A8	ϕV1	Vertical CCD phase 1	
A9	VDD	Output Amplifier Supply	
A10	VLG	Amplifier Load Gate	
A11	RD	Reset Drain	
A12	OG	Output Gate	
A13	ϕH2	Horizontal CCD phase 2 (bot.)	1, 4
B1	GND	Ground	
B2	ϕH1	Horizontal CCD phase 1 (top)	1, 5
B3	ϕR	Reset Clock Video 2	2
B4	VSS	Output Amplifier Return	
B5	VOUT2	Video Output 2	
B6	ϕV2	Vertical CCD phase 2	
B7	GND	Ground	
B8	ϕV2	Vertical CCD phase 2	
B9	VOUT4	Video Output 4	
B10	VSS	Output Amplifier Return	
B11	ϕR	Reset Clock Video 4	2
B12	ϕH1	Horizontal CCD phase 1 (bot.)	1, 6
B13	GND	Ground	

Pin	Label	Function	Notes
C1	VSUB	Substrate	
C2	ϕH1	Horizontal CCD phase 1 (top)	1, 5
C3	ϕR	Reset Clock Video 1	2
C4	VSS	Output Amplifier Return	
C5	VOUT1	Video Output 1	
C6	ϕV2	Vertical CCD phase 2	
C7	GND	Ground	
C8	ϕV2	Vertical CCD phase 2	
C9	VOUT3	Video Output 3	
C10	VSS	Output Amplifier Return	
C11	ϕR	Reset Clock Video 3	2
C12	ϕH1	Horizontal CCD phase 1 (bot.)	1, 6
C13	VSUB	Substrate	
D1	ϕH2	Horizontal CCD phase 2 (top)	1, 3
D2	OG	Output Gate	
D3	RD	Reset Drain	
D4	VLG	Amplifier Load Gate	
D5	VDD	Output Amplifier Supply	
D6	ϕV1	Vertical CCD phase 1	
D8	ϕV1	Vertical CCD phase 1	
D9	VDD	Output Amplifier Supply	
D10	VLG	Amplifier Load Gate	
D11	RD	Reset Drain	
D12	OG	Output Gate	
D13	ϕH2	Horizontal CCD phase 2 (bot.)	1, 4

1. To ensure optimum balancing of the video outputs all HCCD clock edges should arrive at the input pins simultaneously.
2. To ensure optimum balancing of the video outputs all ϕR clock edges should arrive at the input pins simultaneously.
3. Pins A1 and D1 (ϕH2 top) must be connected together.
4. Pins A13 and D13 (ϕH2 bottom) must be connected together.
5. Pins B2 and C2 (ϕH1 top) must be connected together.
6. Pins B12 and C12 (ϕH1 bottom) must be connected together.

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3.1 Absolute Maximum Ratings

		Min.	Max.	Units	Notes
Temperature	Operation without damage	-50	70	C	
	Storage	-55	70	C	
Voltage between pins	VSUB to GND	8	20	V	1
	VDD, VLG, OG, VSS to GND	0	17	V	
	VRD to GND	0	14	V	
	ϕV1 to ϕV2	-20	20	V	
	ϕH1 to ϕH2	-15	15	V	
	ϕR to GND	-15	15	V	
	ϕH1, ϕH2 to OG	-15	15	V	
	ϕH1, ϕH2 to ϕV1, ϕV2	-15	15	V	
Current	Video Output Bias Current	0	10	mA	2

1. For electronic shuttering VSUB may be pulsed to 50 V for up to 10 µs.
2. For each output. Note that the current bias effects the amplifier bandwidth.

Caution: This device contains limited protection against Electrostatic Discharge (ESD).
Devices should be handled in accordance to strict ESD procedures for Class 1 devices.

Caution: Improper cleaning of the cover glass may damage these devices.
Refer to Application Note DS 00-009 "Cover Glass Cleaning Procedure for Image Sensors"

3.2 DC Operating Conditions

Symbol	Description	Min.	Nom.	Max	Units	Notes
OG	Output Gate	1.0	1.5	2.0	V	
VRD	Reset Drain	10.0	10.5	11.0	V	
VSS	Output Amplifier Return		0.0		V	
VLG	Output Amplifier Load Gate	1.2	1.8	2.4	V	
VDD	Output Amplifier Supply	14.5	15.0	15.5	V	
GND	Ground, P-well		0.0		V	
VSUB	Substrate	8.0	TBD	17.0	V	
VESD	ESD Protection	-9.5	-9.0	-8.5	V	1

1. VESD must be at least 1 V more negative than ϕH1L and ϕH2L during sensor operation *AND* during camera power turn-on.

3.3 AC Clock Level Conditions

Symbol	Description	Min.	Nom.	Max.	Units	Notes
ϕV2H	Vertical CCD Clock High	7.5	8.0	8.5	V	
ϕV1M, ϕV2M	Vertical CCD Clocks Midlevel	-1.5	-1.0	-0.8	V	
ϕV1L, ϕV2L	Vertical CCD Clocks Low	-9.5	-9.0	-8.5	V	
ϕH1H, ϕH2H	Horizontal CCD Clocks High	2.5	3.0	4.0	V	
ϕH1L, ϕH2L	Horizontal CCD Clocks Low	-7.5	-7.0	-6.0	V	
ϕR	Reset Clock Amplitude		5.0		V	
ϕRL	Reset Clock Low	1.5	2.0	2.5	V	
VShutter	Electronic Shutter Voltage	44	48	52	V	

3.4 Clock Capacitance

Clocks	Capacitance	Units	Notes
ϕV1 to GND	47	nF	1
ϕV2 to GND	48	nF	1
ϕV1 to ϕV2	5	nF	
ϕH1 to GND	170	pF	1
ϕH2 to GND	188	pF	1
ϕH1 to ϕH2	30	pF	
ϕR to GND	10	pF	

- Capacitance is total for all pins of the same type.

1. Gate capacitance to GND is voltage dependent. Value is for nominal clock voltages.

3.5 AC Timing Conditions

Symbol	Description	Min.	Nom.	Max.	Units	Notes
T_{HD}	HCCD Delay	1.0	1.3	10.0	µs	
T_{VCCD}	VCCD Transfer time	1.3	1.6		µs	
T_{V3rd}	Photodiode Transfer time	8.0	12.0	15.0	µs	
T_{3P}	VCCD Pedestal time	30.0	40.0	60.0	µs	
T_{3D}	VCCD Delay	15.0	20.0	100.0	µs	
T_R	Reset Pulse time	5.0	10.0		ns	
T_S	Shutter Pulse time	2.0	4.0	10.0	µs	
T_{SD}	Shutter Pulse delay	1.0	1.6	10.0	µs	
T_H	HCCD Clock Period	25.0	50.0	200.0	ns	
T_{VR}	VCCD rise/fall time	0.0	0.1	1.0	µs	

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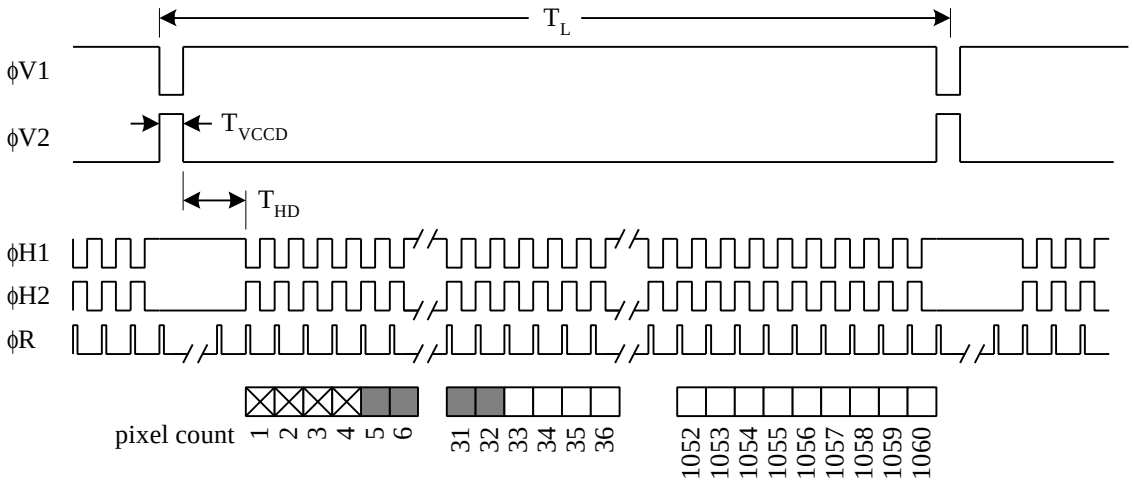
Line Timing



Frame Timing

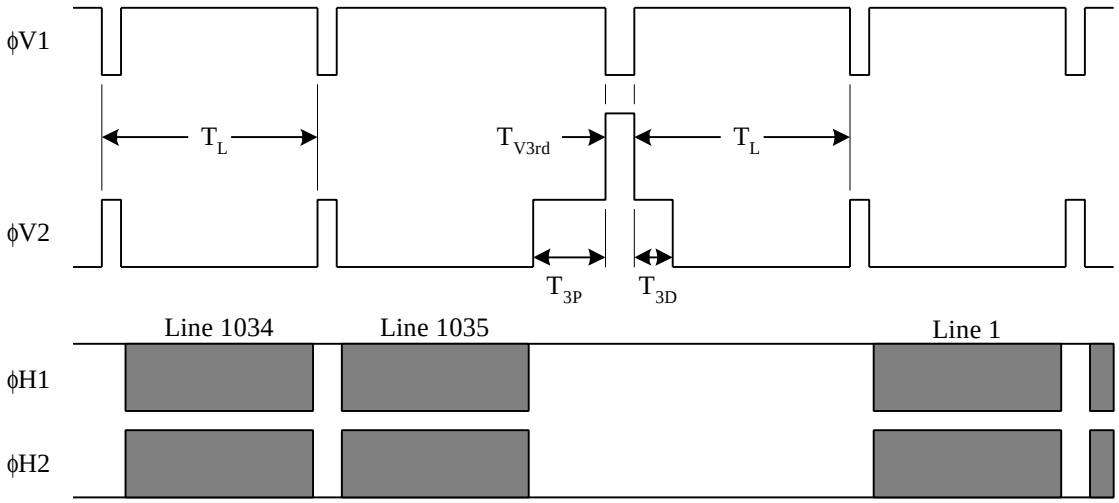


Figure 4 - Timing Diagrams

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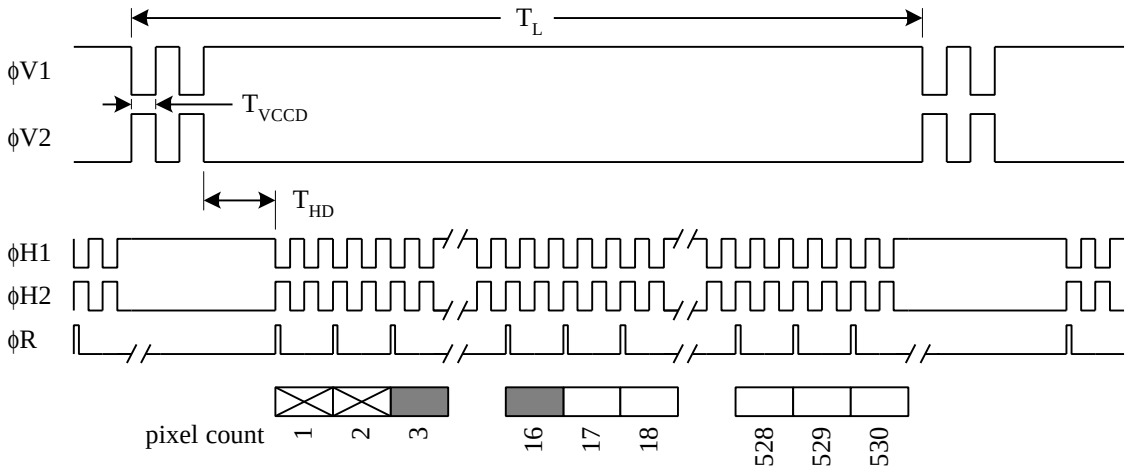
Line Timing - 2 x 2 Binning



Frame Timing - 2 x 2 Binning

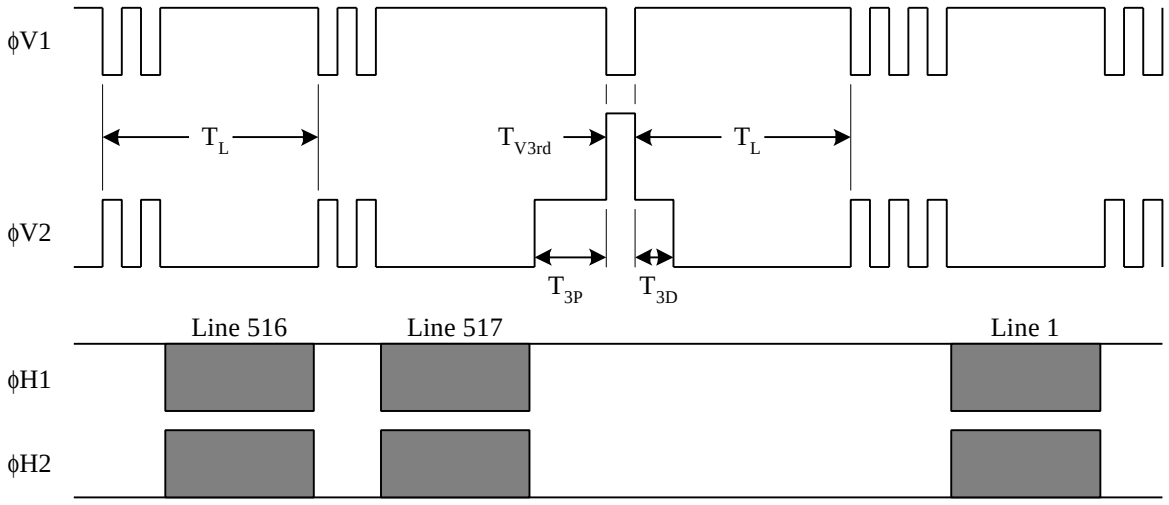


Figure 5 - Timing Diagrams - 2 x 2 Binning

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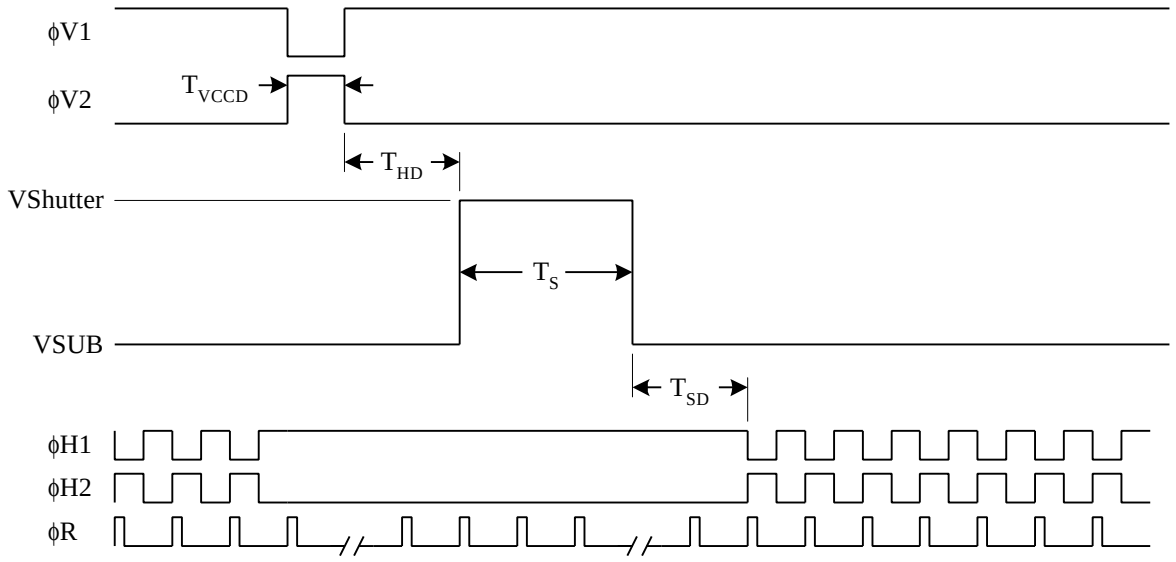
Electronic Shutter Line Timing



Integration Time Definition

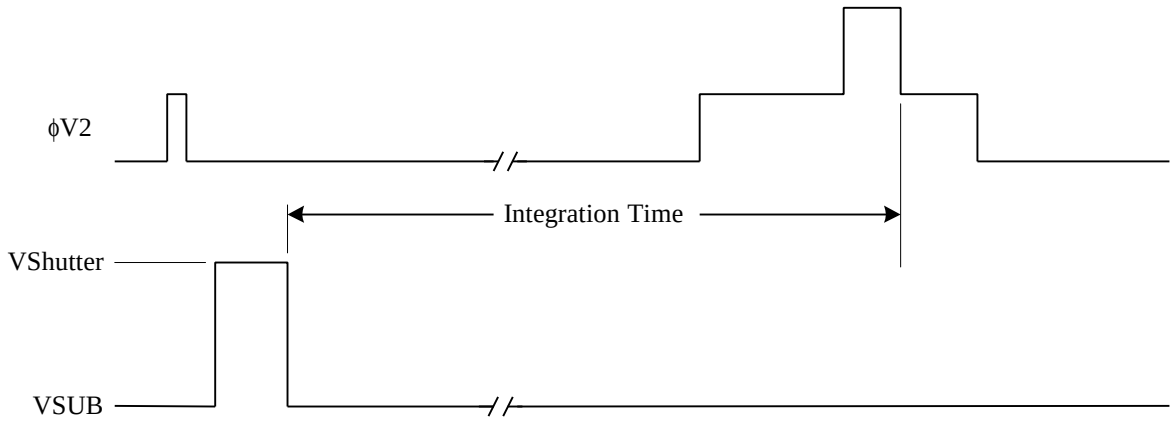


Figure 6 - Electronic Shutter Timing Diagram

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4.1 Performance Specifications

Performance Test Conditions

Temperature	40 °C
Integration Time	67 ms (20 MHz HCCD frequency, no binning, 15 fps frame rate)
Operation	Nominal voltages and timing
Image defects are excluded from performance tests.	

Optical Specifications

Symbol	Description	Min.	Nom.	Max.	Units	Notes
QE_{max}	Peak Quantum Efficiency	33	36		%	
λQE	Peak Quantum Efficiency Wavelength		490		nm	
θQE*h*	Microlens Acceptance Angle (horizontal)	±12	±13		degrees	1
θQE*v*	Microlens Acceptance Angle (vertical)	±25	±30		degrees	1
QE(540)	Quantum Efficiency at 540nm	31	33		%	
NL	Maximum Photoresponse Nonlinearity		2		%	2, 3
ΔG	Maximum Gain Difference Between Outputs		10		%	2, 3
ΔNL	Maximum Signal Error caused by Nonlinearity Differences		1		%	2, 3

1. Value is the angular range of incident light for which the quantum efficiency is at least 50% of QE_{max} at a wavelength of λQE. Angles are measured with respect to the sensor surface normal in a plane parallel to the horizontal axis (θQE*h*) or in a plane parallel to the vertical axis (θQE*v*).
2. Value is over the range of 10% to 90% of photodiode saturation.
3. Value is for the sensor operated without binning.

CCD Specifications

Symbol	Description	Min	Nom.	Max.	Units	Notes
VNe	Vertical CCD Charge Capacity	50	55		ke^-	
HNe	Horizontal CCD Charge Capacity	220	250		ke^-	
PNe	Photodiode Charge Capacity	35	40		ke^-	1
Id	Dark Current		0.2	0.8	nA/cm^2	
Lag	Image Lag		< 10	50	e^-	2
Xab	Antiblooming factor	100	300			3, 4, 5, 6
Smr	Vertical Smear		-75	-72	dB	3, 4

1. This value depends on the substrate voltage setting. Higher photodiode saturation charge capacities will lower the antiblooming specification. Substrate voltage will be specified with each part for nominal photodiode charge capacity.
2. This is the first field decay lag at 70% saturation. Measured by strobe illumination of the device at 70% of photodiode saturation, and then measuring the subsequent frame's average pixel output in the dark.
3. Measured with F/4 imaging optics and continuous green illumination centered at 550 nm.
4. Measured with a spot size of 100 vertical pixels.
5. A blooming condition is defined as when the spot size doubles in size.
6. Antiblooming factor is the light intensity which causes blooming divided by the light intensity which first saturates the photodiodes.

Output Amplifier Specifications

Symbol	Description	Nominal	Units	Notes
P_d	Power Dissipation		mW	1
F_{-3dB}	Bandwidth	140	MHz	1
C_L	Max Off-chip Load	10	pF	2
A_v	Gain	0.75		1
$\Delta V/\Delta N$	Sensitivity	12	$\mu V/ e^-$	1

1. For a 5 mA output load on each output amplifier, with nominal output amplifier voltages VDD, VLG and VSS.
2. With total output load capacitance of C_L= 10 pF between the outputs and AC ground.

General Specifications

Symbol	Description	Nominal	Units	Notes
n_{e-T}	Total Noise	40	e^- rms	1
DR	Dynamic Range	60	dB	2

1. Includes system electronics noise, dark pattern noise and dark current shot noise.
2. Uses 20LOG(PNe/n_{e-T})

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4.2 Typical Quantum Efficiency

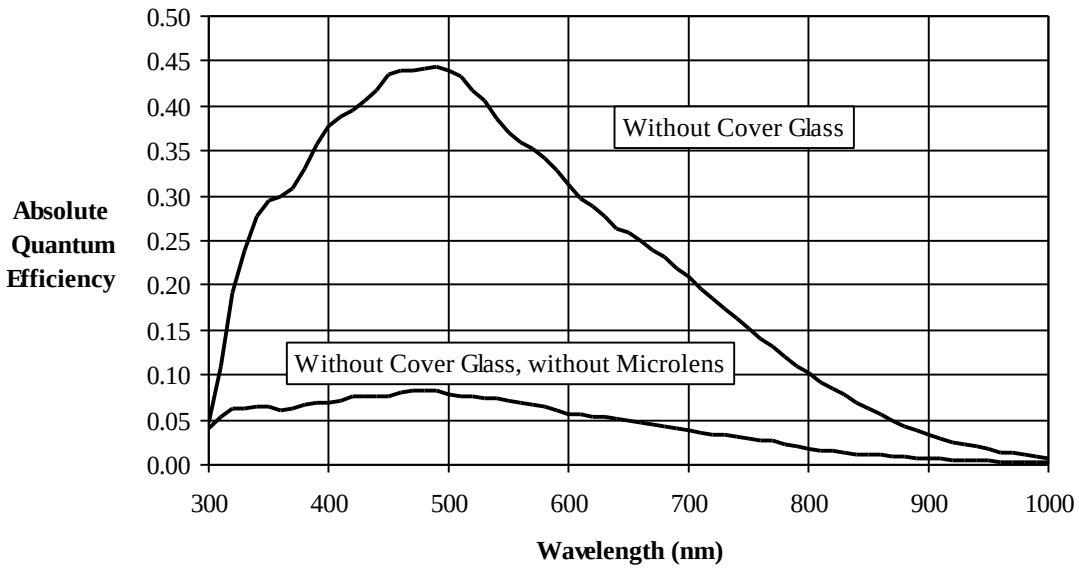

Figure 7 - Wavelength Dependence of Quantum Efficiency

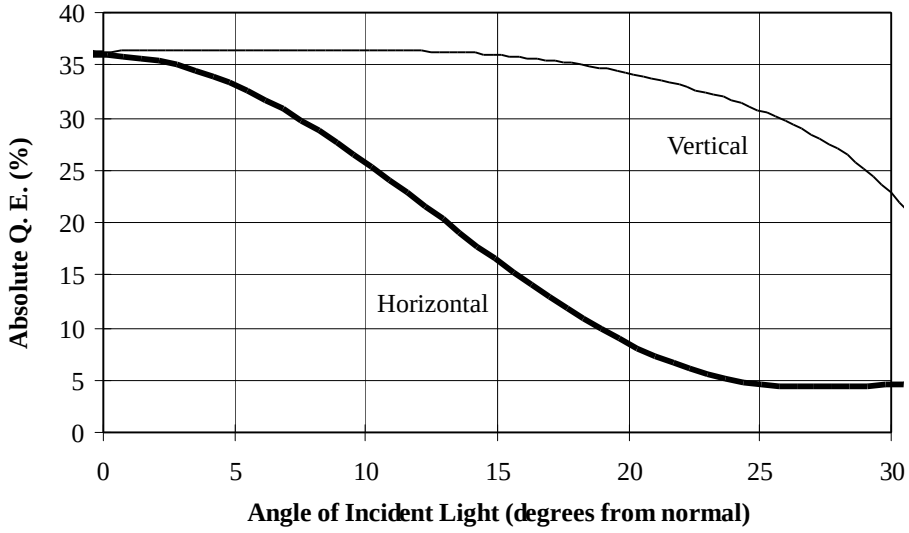

Figure 8 - Angular Dependence of Quantum Efficiency

For the curve marked "Horizontal", the incident light angle is varied in a plane parallel to the HCCD.
For the curve marked "Vertical", the incident light angle is varied in a plane parallel to the VCCD.

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4.3 Operation Notes

Exposure Control
When the sensor is operated with a 20 MHz horizontal CCD frequency, the frame rate is 15 fps and the integration time is 67 ms. To achieve shorter integration times, the electronic shutter option may be used by applying a pulse to the substrate. The time between the falling edge of the substrate pulse and the falling edge of the ϕV2 clock from ϕV2H to ϕV2M is defined as the integration time. The substrate pulse and integration time are shown in Fig. 6.

Integration times longer than one frame time do not require use of the electronic shutter. Without the electronic shutter the integration time is defined as the time between successive pulses of the ϕV2 clock to the ϕV2H level. When the ϕV2 clock is at the ϕV2H level, charge collected in the photodiodes is transferred to the vertical shift register. To extend the integration time, increase the time between each ϕV2H level of the ϕV2 clock. While the photodiodes are integrating photoelectrons the vertical and horizontal shift registers should be continuously clocked to prevent the collection of dark current in the vertical shift register. This is most easily done by increasing the number of lines read out of the image sensor. For example, to double the integration time read out 2070 lines instead of 1035 lines (but remember only the first 1035 lines will contain charge from photodiodes).

Depending on the image quality desired and temperature of the sensor, integration times longer than one second may require the sensor to be cooled to reduce dark current. The heat from the output amplifiers will also generate a non-uniform dark current pattern near the bottom corners of the sensor. This can be reduced at long integration times by turning on VDD to each amplifier only during image readout. If the vertical and horizontal shift registers are also stopped during integration time, the dark current in the shift registers should be flushed out completely before transferring charge from the photodiodes to the vertical shift register.

Dark References
There are 28 light shielded columns at the left and right side of the image sensor. The first and last light shielded columns should not be used due to some light leakage under the edges of the light shielding. Only the center 26 columns should be used for dark reference line clamping. There are 7 light shielded rows at the top and bottom of the image sensor. Only rows 5 and 6 of the light shielded rows should be used as a dark reference.

Connections to the Image Sensor
The reset clock operates at the pixel frequency. The traces on the circuit board to the reset clock pins should be kept short and of equal length to ensure that the reset pulse arrives at each pin simultaneously. The circuit board traces to the horizontal clock pins should also be designed to ensure that the clock edges arrive at each pin simultaneously. If reset pulses and the horizontal clock edges are misaligned the noise performance of the sensor will be degraded and balancing the offset and gain of the four output amplifiers will be difficult.

The bias voltages on OG, RD, VSS, VLG and VDD should be well filtered with capacitors placed as close to the pins as possible. Noise on the video outputs will be most strongly effected by noise on VSS, VLG, VDD, GND, and VSUB. If the electronic shutter is not used then a filtering capacitor should also be placed on VSUB. If the electronic shutter is used, the VSUB voltage should be kept as clean and noise free as possible.

The ESD voltage must reach its operating point before any of the horizontal clocks reach their low level. If any voltage on the sensor comes within 1 V of the ESD voltage, the electrostatic damage protection circuit will become active and will not turn off until all voltages are removed. Operating the sensor with the ESD protection circuit active may damage the sensor.

4.4 Defect Specifications

Defect Test Conditions

Temperature	40°C
Integration Time	67 ms (20 MHz HCCD frequency, no binning, 15 fps frame rate)
Light source	Continuous green illumination centered at 550 nm
Operation	Nominal voltages and timing

Defect Definitions

Name	Maximum Number	Definition
Local Average	-	Average over a 100 by 100 pixel region surrounding the pixel of interest.
Major Defective Pixel	100	A pixel whose signal deviates by more than 25 mV from the local average at zero illumination or a pixel whose signal deviates by more than 15% from the local average under uniform illumination at 80% of saturation
Minor Defective Pixel	200	A pixel whose signal deviates by more than 8 mV from the local average at zero illumination
Major Cluster	4	A group of 5 to 8 contiguous defective pixels, but no more than 2 adjacent defects horizontally
Minor Cluster	16	A group of 2 to 4 contiguous defective pixels, but no more than 2 adjacent defects horizontally
Column	0	A group of 10 or more contiguous defective pixels in a single column

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5.1 Quality Assurance and Reliability

5.1.1 Quality Strategy: All devices will conform to the specifications stated in this document. This is accomplished through a combination of statistical process control and inspection at key points of the production process.

5.1.2 Replacement: All devices are warranted against failures in accordance with the Terms of Sale.

5.1.3 Cleanliness: Devices are shipped free of contamination, scratches, etc. that would cause a visible defect.

5.1.4 ESD Precautions: Devices are shipped in static-safe containers and should only be handled at static-safe work stations.

5.1.5 Reliability: Information concerning the quality assurance and reliability testing procedures and results are available from the Microelectronics Technology Division, and can be supplied upon request.

5.1.6 Test Data Retention: Devices have an identifying number traceable to a test data file. Test data is kept for a period of 2 years after date of shipment.

5.2 Ordering Information

See Appendix 1 for available part numbers.

Address all inquiries and purchase orders to:

Image Sensor Solutions
Eastman Kodak Company
Rochester, New York 14650-2010
Phone: (716) 722-4385
Fax: (716) 477-4947
E-mail: ccd@kodak.com

Kodak reserves the right to change any information contained herein without notice. All information furnished by Kodak is believed to be accurate.

WARNING: LIFE SUPPORT APPLICATIONS POLICY

Kodak image sensors are not authorized for and should not be used within Life Support Systems without the specific written consent of the Eastman Kodak Company. Product warranty is limited to replacement of defective components and does not cover injury or property or other consequential damages.

Appendix 1 Part Number Availability

Note:

This appendix may be updated independently of the performance specification. Contact Eastman Kodak for the latest revision.

Device Name	Available Part Numbers	Features		
KAI-4000M	2H4822	Monochrome	Microlens	Sealed
KAI-4000M	2H4819	Monochrome	Microlens	Taped Cover Glass
KAI-4000	2H4813	Monochrome	-	Taped Cover Glass