KAF - 1301LE

1280 (H) x 1024 (V) Pixel

Full-Frame CCD Image Sensor

Performance Specification

Eastman Kodak Company

Microelectronics Technology Division

Rochester, New York 14650-2010

Revision B
June 7, 1999

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TABLE OF CONTENTS

APPENDIX

FIGURES

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1.1 Features

1.3M Pixel Area CCD

1280H x 1024V (16 mm) Pixels

Transparent Gate True Two Phase Technology (Enhanced Spectral Response)

20.248mm H x 16.38mm V Photosensitive Area

2-Phase Register Clocking

Anti-blooming Protection

70% Fill Factor

Low Dark Current (<30pA/cm^2 @ 25^{o}C

1.2 Description

The KAF-1301LE is a high performance monochrome area CCD (charge-coupled device) image sensor with 1280H x 1024V photoactive pixels designed for a wide range of image sensing applications in the 0.4 nm to 1.0 nm wavelength band. Typical applications include military, scientific, and industrial imaging. A 75dB dynamic range is possible when operating at room temperature.

The sensor is built with a true two-phase CCD technology. This technology simplifies the support circuits that drive the sensor and reduces the dark current without compromising charge capacity. The transparent gate results in spectral response increased ten times at 400nm, compared to a front side illuminated standard poly silicon gate technology. The sensitivity is increased 50% over the rest of the visible wavelengths.

Total chip size is 22mm x 17.1mm and is housed in a 36-pin package with an integral copper-tungsten back plate providing excellent thermal conductivity.

The sensor consists of 1296 parallel (vertical) CCD shift registers each 1028 elements long. These registers act as both the photosensitive elements and as the transport circuits that allow the image to be sequentially read out of the sensor. The elements of these registers are arranged into a 1280 x 1024 photosensitive array surrounded by a light shielded dark reference of 16 columns and 4 rows. Parallel (vertical) CCD registers transfer the image one line at a time into a single 1304 element (horizontal) CCD shift register. The horizontal register transfers the charge to a single output amplifier. The output amplifier is a two-stage source follower that converts the photo-generated charge to a voltage for each pixel.

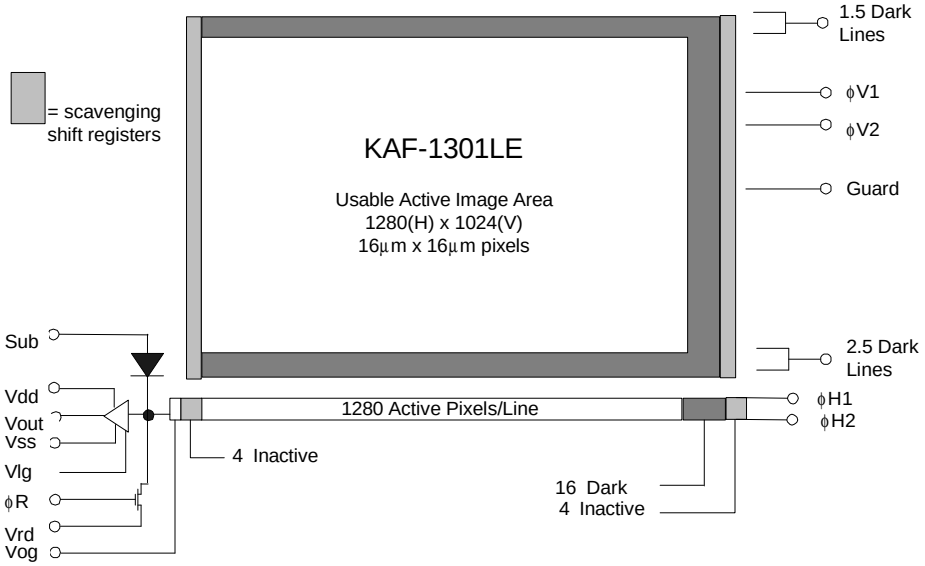

Figure 1 - Functional Block Diagram

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1.3 Image Acquisition

An electronic representation of an image is formed when incident photons falling on the sensor plane create electron-hole pairs within the sensor. These photon-induced electrons are collected locally by the formation of potential wells at each photogate or pixel site. The number of electrons collected is linearly dependent on light level and exposure time and non-linearly dependent on wavelength. When the pixel's capacity is reached, excess electrons are removed by the presence of a lateral overflow drain (LOD) anti-blooming protection structure. During the integration period, the ϕV1and ϕV2 register clocks are held at a constant (low) level.
See Figure 5 - Timing Diagrams.

1.4 Charge Transport

Referring again to Figure 5 - Timing Diagrams, the integrated charge from each photogate is transported to the output using a two step process. Each line (row) of charge is first transported from the vertical CCDs to the horizontal CCD register using the ϕV1and ϕV2 register clocks. The horizontal CCD is presented a new line on the falling edge of ϕV2 while ϕH1 is held high. The horizontal CCDs then transport each line, pixel by pixel, to the output structure by alternately clocking the ϕH1 and ϕH2 pins in a complementary fashion. On each falling edge of ϕH1 a new charge packet is transferred onto a floating diffusion and sensed by the output amplifier.

1.5 Output Structure

Charge presented to the floating diffusion (FD) is converted into a voltage and current amplified in order to drive off-chip loads. The resulting voltage change seen at the output is linearly related to the amount of charge placed on FD. Once the signal has been sampled by the system electronics, the reset gate (ϕ_R) is clocked to remove the signal and FD is reset to the potential applied by VRD. More signal at the floating diffusion reduces the voltage seen at the output pin. In order to activate the output structure, an off-chip load must be added to the Vout pin of the device - see Figure 4. The amplifier has a 45MHz bandwidth.

1.6 Dark Reference Pixels

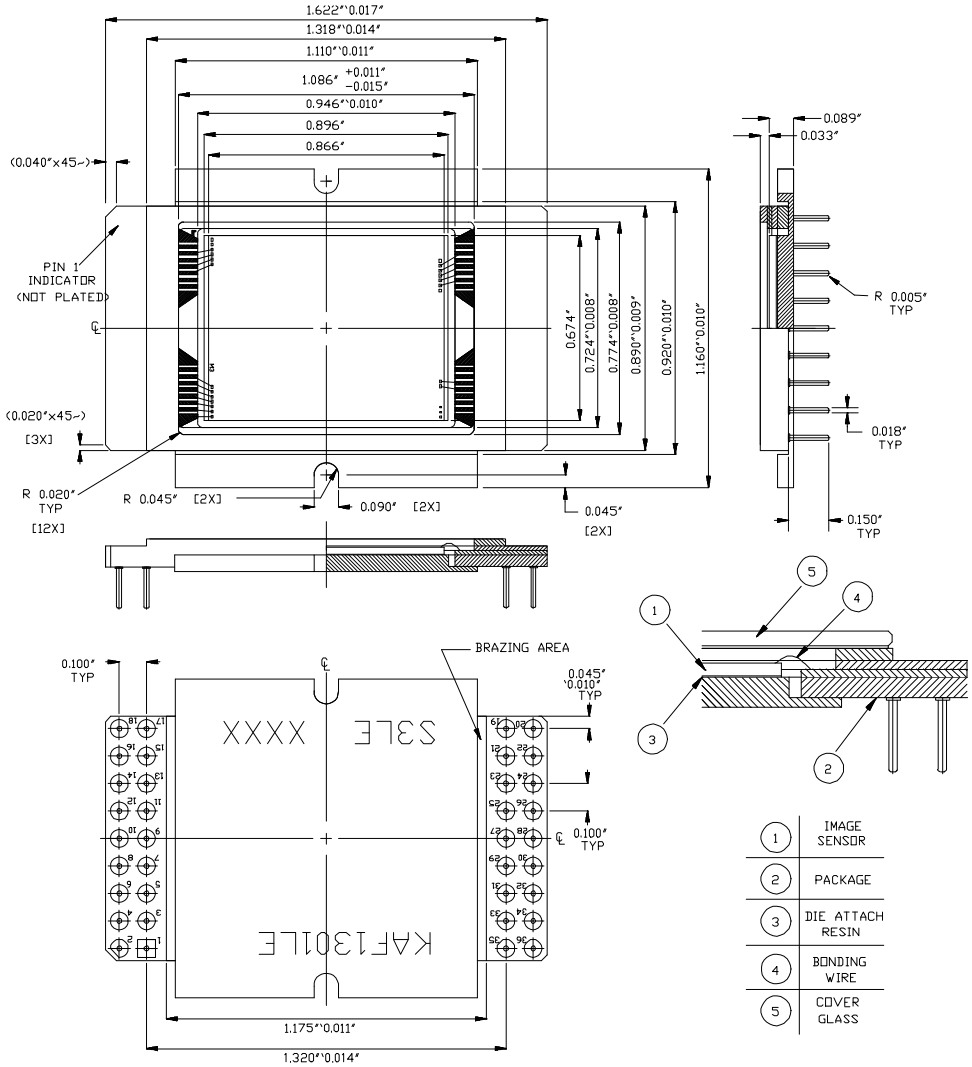
Surrounding the peripheral of the device is a border of light shielded pixels. These can be used to track the dark level if the temperature of the array is allowed to vary. Each line has 16 trailing pixels that are connected to vertical CCD registers covered with aluminum. There are also 2.5 dark lines at the start of every frame and 1.5 dark lines at the end of each frame. That is, the light shield covering the dark reference rows extend into the adjacent photo-active row. This provides better rejection of unwanted optical signal at the expense of lower response in the adjacent photo active rows. Under normal circumstances, these pixels do not respond to light. However, dark reference pixels in close proximity to an active pixel, or the outer bounds of the chip (including the first two lines out), can scavenge signal depending on light intensity and wavelength and therefore will not represent the true dark signal.

1.7 Dummy Pixels

Within the horizontal shift register are 4 leading and 4 trailing additional shift phases which are not associated with a column of pixels within the vertical register. These pixels contain only horizontal shift register dark current signal and do not respond to light. A few leading dummy pixels may scavenge false signal depending on operating conditions.

There are several columns of dummy vertical CCD adjacent to the photo active and light shielded vertical CCD that act to scavenge unwanted stray signal away from the imaging area. These columns are not connected to the horizontal register so their presence does not have to be taken into account when clocking out each line. They transfer their charge in a direction opposite of the photo-active columns and the charge is removed through a connection to Vdd.

2.1 Package Configuration



Detailed drawings available upon request.

Figure 2 - Package Drawing

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2.2 Pin Description

Pin	Symbol	Description	Pin	Symbol	Description
3, 4, 33, 34	ϕ_{V2}	Vertical (Parallel) CCD Clock - Phase 2	16	VLG	Amplifier Load Gate
5, 6, 31, 32	ϕ_{V1}	Vertical (Parallel) CCD Clock - Phase 1	17	VOUT	Video Output
2	VLOD	Overflow drain bias	18	VDD	Amplifier Supply
12	VOG	Output Gate	23	ϕ_{H1}	Horizontal CCD Clock - Phase 1
13	ϕR	Reset Clock	24	ϕ_{H2}	Horizontal CCD Clock - Phase 2
14	VRD	Reset Drain	30	VSUB	Substrate (Ground)
15	VSS	Amplifier Supply Return	all others	N/C	No Connection (open pin)

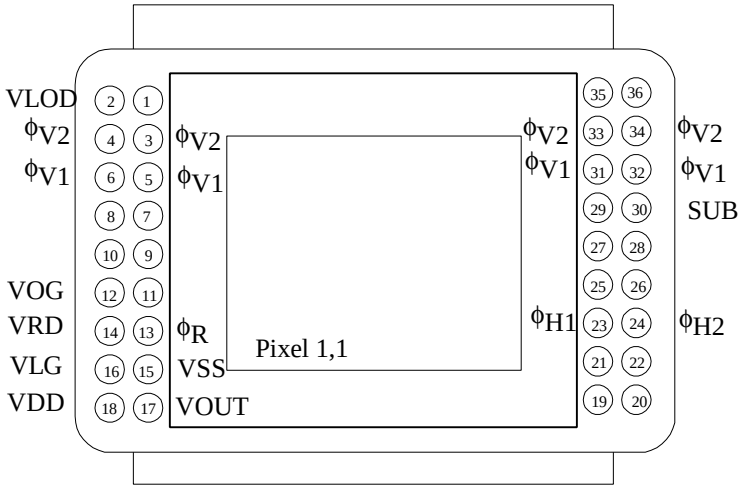

Figure 3 - Packaging Pin Designations

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3.1 Absolute Maximum Ratings

Description	Symbol	Min.	Max.	Units	Notes
Diode Pin Voltages	Vdiode	0	20	V	1, 2
Gate Pin Voltages - Type 1	Vgate1	-16	16	V	1, 3
Gate Pin Voltages - Type 2	Vgate2	0	16	V	1, 4
Inter-Gate Voltages	Vg-g		16	V	5
Output Bias Current	Iout		-10	mA	6
Output Load Capacitance	Cload		15	pF	6
Storage Temperature	T		100	°C	
Humidity	RH	5	90	%	7

Notes:
1. Referenced to pin VSUB.
2. Includes pins: VRD, VDD, VSS, VOUT.
3. Includes pins: ϕV1, ϕV2, ϕH1, ϕH2.
4. Includes pins: VOG, VLG, ϕR
5. Voltage difference between overlapping gates. Includes: ϕV1 to ϕV2, ϕH1 to ϕH2, ϕV2 to ϕH1, ϕH2 to VOG.
6. Avoid shorting output pins to ground or any low impedance source during operation.
7. T=25°C. Excessive humidity will degrade MTTF.

Caution: This device contains limited protection against Electrostatic Discharge (ESD).
Devices should be handled in accordance with strict ESD protective procedures for Class 1 devices.

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3.2 DC Operating Conditions

Description	Symbol	Min.	Nom.	Max.	Units	Max. DC Current (mA)	Notes
Reset Drain	VRD	10.5	11.0	11.25	V	0.01	
Output Amplifier Return	VSS	1.5	2.0	2.5	V	-0.5	
Output Amplifier Supply	VDD	14.5	15	15.5	V	Iout	
Amplifier load gate	VLG	Vss + 0.0	Vss +1.0	Vss+1 .5	V	0.01	
Substrate	VSUB	0	0	0	V	0.01	
Antiblooming drain	VLOD	8	9	15			1
Output Gate	VOG	3.75	4	5	V	0.01	
Video Output Current	Iout		-5	-10	mA	-	2

Notes:
1. If this pin is left floating then an internal bias will set VLOD to +15 volts. An external bias can be applied to lower this potential. The dark current at reduced temperatures has been observed to depend on this bias and is optimal with VLOD = 9 volts. The dark current may be higher when the VLOD is greater than 12 volts and the temperature reduced to < -10ºC.
2. An output load sink must be applied to Vout to activate output amplifier - see Figure below.

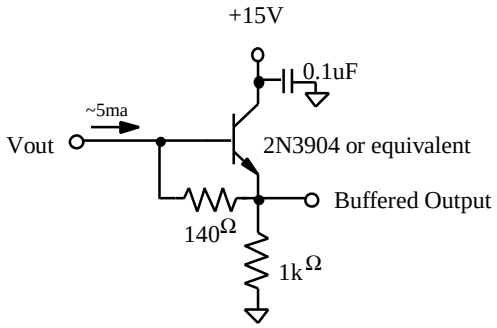


Figure 4 - Recommended Output Structure Load Diagram

3.3 AC Operating Conditions

Description	Symbol	Level	Min.	Nom.	Max.	Units	Effective Capacitance	Notes
Vertical CCD Clock - Phase 1	ϕV1	Low High	-10.5 0	-10.0 0.5	-9.5 1.0	V V	24nF (all ϕV1 pins)	
Vertical CCD Clock - Phase 2	ϕV2	Low High	-10.5 0	-10.0 0.5	-9.5 1.0	V V	24nF (all ϕV2 pins)	
Horizontal CCD Clock - Phase 1	ϕH1	Low High	-2.5 7.5	-2.0 8.0	-1.75 8.5	V V	100pF	
Horizontal CCD Clock - Phase 2	ϕH2	Low High	-2.5 7.5	-2.0 8.0	-1.75 8.5	V V	100pF	
Reset Clock	ϕR	Low High	1.5 8.5	2.0 9.0	2.5 9.5	V V	5pF	

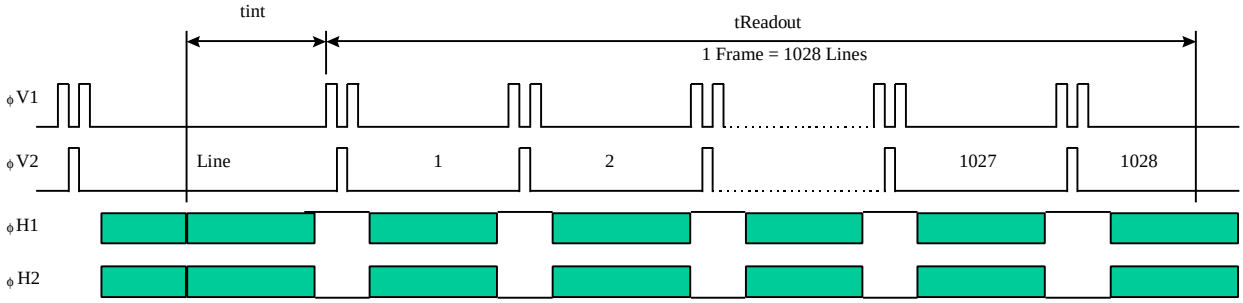
Notes:
1. All pins draw less than 10uA DC current.
2. Capacitance values relative to VSUB.

3.4 AC Timing Conditions

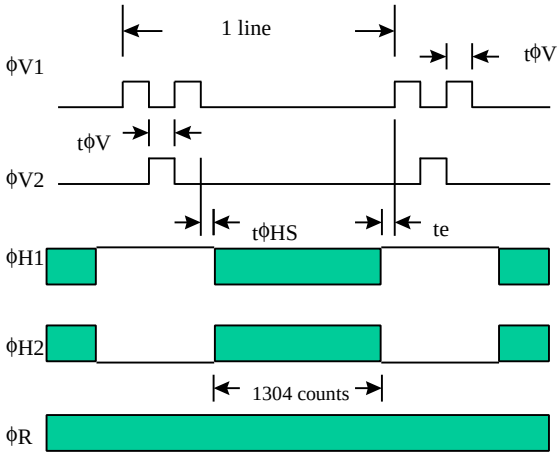
Description	Symbol	Min.	Nom.	Max.	Units	Notes
ϕH1, ϕH2 Clock Frequency	f_H		4	10	MHz	1, 2, 3
ϕV1, ϕV2 Clock Frequency	f_V		142	200	kHz	1, 2, 3
Pixel Period (1 Count)	t_e	100	250		ns	
ϕH1, ϕH2 Setup Time	t_{fHS}	0.5	1		µs	
ϕV1, ϕV2 Clock Pulse Width	t_{fV}	5	7		µs	2
Reset Clock Pulse Width	t_{fR}	10	20		ns	4
Readout Time	$t_{readout}$	156.7	357.7		ms	5
Integration Time	t_{int}					6
Line Time	t_{line}	152.4	348		µs	7

Notes:
1. 50% duty cycle values.
2. CTE may degrade above the nominal frequency.
3. Rise and fall times (10/90% levels) should be limited to 5-10% of clock period. Cross-over of register clocks should be between 40-60% of amplitude.
4. f_R should be clocked continuously.
5. $t_{readout} = (1028 * t_{line})$
6. Integration time is user specified. Longer integration times will degrade noise performance due to accumulated dark signal.
7. $t_{line} = (3 * t\phi_v) + t\phi_{HS} + (1304 * t_e) + t_e$

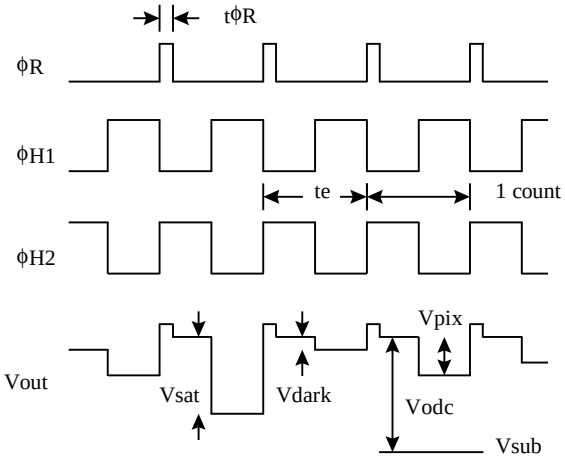
Frame Timing



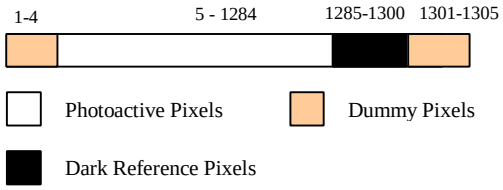
Line Timing Detail



Pixel Timing Detail



Line Content



Vsat Saturated pixel video output signal
Vdark Video output signal in no light situation, not zero due to
Vpix Pixel video output signal level, more electrons =more
Vodc Video level offset with respect to vsub
Vsub Analog Ground

* See Image Aquisition - section 1.3 (page 4)

Figure 5 - Timing Diagrams

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4.1 Performance Specifications

All values measured at 25°C, and nominal operating conditions. These parameters exclude defective pixels.

Description	Symbol	Min.	Nom.	Max.	Units	Notes
Saturation Signal Vertical CCD capacity Horizontal CCD capacity Output Node capacity	Nsat	 120000 280000 190000	 120000 300000 220000	 240000	 electrons / pixel	 1
Red Quantum Efficiency (λ=650nm) Green Quantum Efficiency (λ=550nm) Blue Quantum Efficiency (λ=450nm)	Rr Rg Rb		28 32 20		% % %	
Photoresponse Non-Linearity	PRNL		1	2	%	2
Photoresponse Non-Uniformity	PRNU		1	3	%	3
Dark Signal	Jdark		150 7	330 15	electrons / pixel / sec pA/cm^2	4
Dark Signal Doubling Temperature		5	6.3	7.5	^oC	
Dark Signal Non-Uniformity	DSNU		150	330	electrons / pixel / sec	5
Dynamic Range	DR	72	74		dB	6
Charge Transfer Efficiency	CTE	0.99995	0.99998			
Output Amplifier DC Offset	Vodc	10.5	12	13	V	7
Output Amplifier Bandwidth	f_{-3dB}		45		Mhz	8
Output Amplifier Sensitivity	Vout/Ne~	7	9	11	uV/e~	
Output Amplifier output Impedance	Zout	175	200	250	Ohms	
Noise Floor	ne~		15	20	electrons	9
Anti-blooming suppression	Xab	100				10

Notes:
1. For pixel binning applications, electron capacity up to 330000 can be achieved with modified CCD inputs. Each sensor may have to be optimized individually for these applications. Some performance parameters may be compromised to achieve the largest signals.
2. Worst case deviation from straight line fit, between 1% and 90% of Vsat.
3. One Sigma deviation of a 128x128 sample when CCD illuminated uniformly.
4. Average of all pixels with no illumination at 25°C..
5. Average dark signal of any of 10 x 8 blocks within the sensor. (each block is 128 x 128 pixels)
6. 20log (Nsat / ne~) at nominal operating frequency and 25 °C.
7. Video level offset with respect to ground
8. Last output amplifier stage only. Assumes 10pF off-chip load..
9. Output noise at 25°C , nominal operating frequency, and tint = 0.
10. Number of times above the Vsat illumination level required to cause 10% distortion in a test pattern consisting of a bright circular region approximately 1/20 the size of the image sensor. At this level the sensor does not exhibit classic image sensor blooming but instead a local leakage among adjacent pixels.

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4.2 Typical Performance Characteristics

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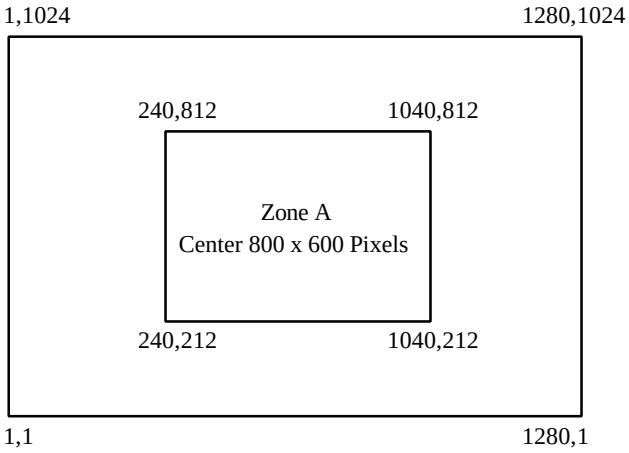
4.3 Defect Classification

Defect tests performed at T=25°C.

Class	Point Defects		Cluster Defects		Column Defects	
	Total	Zone A	Total	Zone A	Total	Zone A
C0	0	0	0	0	0	0
C1	≤5	≤2	0	0	0	0
C2	≤10	≤5	≤4	≤2	≤2	0
C3	≤20	≤10	≤8	≤4	≤4	≤2



Point Defect	DARK: A pixel which deviates by more than 6% from neighboring pixels when illuminated to 70% of saturation, OR BRIGHT: A Pixel with dark current > 5000 e/pixel/sec at 25C.
Cluster Defect	A grouping of not more than 5 adjacent point defects
Column Defect	A grouping of >5 contiguous point defects along a single column, OR A column containing a pixel with dark current > 10,000e/pixel/sec, OR A column that does not meet the minimum vertical CCD charge capacity, OR A column which loses more than 500 e under 2Ke illumination.
Neighboring pixels	The surrounding 128 x 128 pixels or ±64 columns/rows.
Defect Separation	Column and cluster defects are separated by no less than two (2) pixels in any direction (excluding single pixel defects).
Defect Region Exclusion	Defect region excludes the outer two (2) rows and columns at each side/end of the sensor.

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5.1 Quality Assurance and Reliability

5.1.1 Quality Strategy: All devices will conform to the specifications stated in this document. This is accomplished through a combination of statistical process control and inspection at key points of the production process.

5.1.2 Replacement: All devices are warranted against failure in accordance with the terms of Terms of Sale.

5.1.3 Cleanliness: Devices are shipped free of contamination, scratches, etc. that would cause a visible defect.

5.1.4 ESD Precautions: Devices are shipped in a static-safe container and should only be handled at static-safe work stations.

5.1.5 Reliability: Information concerning the quality assurance and reliability testing procedures and results are available from the Microelectronics Technology Division and can be supplied upon request.

5.1.6 Test Data Retention: Devices have an identifying number of traceable to a test data file. Test data is kept for a period of 2 years after date of shipment.

5.2 Ordering Information

See Appendix 1 for available part numbers

Address all inquiries and purchase orders to:

Microelectronics Technology Division
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Kodak reserves the right to change any information contained herein without notice. All information furnished by Kodak is believed to be accurate.

WARNING: LIFE SUPPORT APPLICATIONS POLICY

Kodak image sensors are not authorized for and should not be used within Life Support Systems without the specific written consent of the Eastman Kodak Company.

Product warranty is limited to replacement of defective components and does not cover injury, or property or other consequential damages.

APPENDIX

Appendix 1 – Part number Availability

Device	Part Number	Features
KAF-1301LE	2H4130	Clear Taped Cover Glass, Class 1
KAF-1301LE	2H4131	Clear Taped Cover Glass, Class 2
KAF-1301LE	2H4132	Clear Taped Cover Glass, Class 3
KAF-1301LE	2H4128	Clear Taped Cover Glass, Class 4
KAF-1301LE	2H4133	Clear Taped Cover Glass, Engineering Grade
KAF-1301LE	2H4134	Clear Taped Cover Glass, Mechanical Grade

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