KAF - 1001E

1024(H) x 1024(V) Pixel

Enhanced Response

Full-Frame CCD Image Sensor

Performance Specification

Eastman Kodak Company

Microelectronics Technology Division

Rochester, New York 14650

Revision 0
August 24, 1999

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1.1 Features

- **Front Illuminated Full-Frame Architecture with Blue Plus Transparent Gate True Two Phase Technology for high sensitivity**
- **1024(H) x 1024(V) Photosensitive Pixels**
- **24µm(H) x 24µm(V) Pixel Size**
- **24.5 mm x 24.5 mm Photo active Area**
- **1:1 Aspect Ratio**
- **100% Fill Factor**
- **Single Readout Register**
- **2 Clock Selectable Outputs**
- **High Gain Output (11 µV/e⁻) for low noise**
- **Low Gain Output (2.0 µV/e⁻) for high dynamic range**
- **Low Dark Current (<30 pA/cm^2 @ T=25^{o}C)**

1.2 Description

The KAF-1001E is a high-performance, silicon charge-coupled device (CCD) designed for a wide range of image sensing applications in the 0.4mm to 1.1mm wavelength band.

Common applications include medical, scientific, military, machine and industrial vision.

The sensor is built with a true two-phase CCD technology employing a transparent gate. This technology simplifies the support circuits that drive the sensor and reduces the dark current without compromising charge capacity. The transparent gate results in spectral response increased ten times at 400nm, compared to a front side illuminated standard polysilicon gate technology. The sensitivity is increased 50% over the rest of the visible wavelengths.

The clock selectable on-chip output amplifiers have been specially designed to meet two different needs. The first is a high sensitivity 2-stage output with 11µV/e$^-$ charge to voltage conversion ratio. The second is a single-stage output with 2µV/e- charge to voltage conversion ratio.

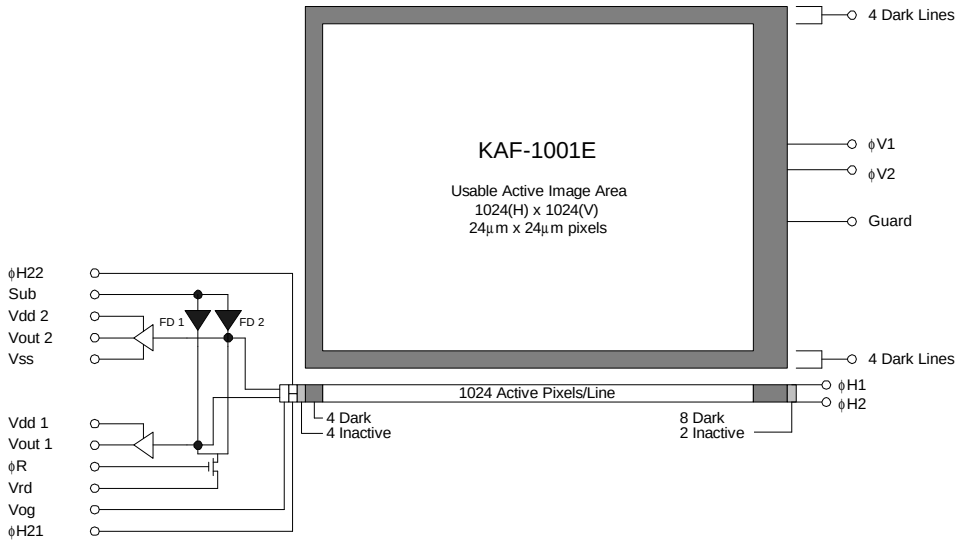

Figure 1 - Functional Block Diagram

(Shaded areas represent 4 non-imaging pixels at the beginning and 8 non-imaging pixels at the end of each line. There are also 4 non-imaging lines at the top and bottom of each frame.)

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1.3 Architecture

Refer to the block diagram in Figure 1. The KAF-1001E consists of one vertical (parallel) CCD shift register, one horizontal (serial) CCD shift register and a selectable high or low gain output amplifier. Both registers incorporate true two-phase buried channel technology. The vertical register consists of 24µm x 24µm photo-capacitor sensing elements (pixels) which also serves as the transport mechanism. The pixels are arranged in a 1024(H) x 1024(V) array; an additional 12 columns (4 at the left and 8 at the right) and 8 rows (4 each at top and bottom) of non-imaging pixels are added as dark reference. Because there is no storage array, this device must be synchronized with strobe illumination or shuttered during readout.

1.4 Image Acquisition

An image is acquired when incident light, in the form of photons, falls on the array of pixels in the vertical CCD register and creates electron-hole pairs (or simply electrons) within the silicon substrate. This charge is collected locally by the formation of potential wells created at each pixel site by induced voltages on the vertical register clock lines (ϕV1, ϕV2). These same clock lines are used to implement the transport mechanism as well. The amount of charge collected at each pixel is linearly dependent on light level and exposure time and non-linearly dependent on wavelength until the potential well capacity is exceeded. At this point charge will 'bloom' into vertically adjacent pixels.

1.5 Charge Transport

Integrated charge is transported to the output in a two step process. Rows of charge are first shifted line by line into the horizontal CCD. 'Lines' of charge are then shifted to the output pixel by pixel. Referring to the timing diagram, integration of charge is performed with ϕV1 and ϕV2 held low. Transfer to horizontal CCD begins when ϕV1 is brought high causing charge from the ϕV1 and ϕV2 gates to combine under the ϕV1 gate. ϕV1 and ϕV2 now reverse their polarity causing the charge packets to 'spill' forward under the ϕV2 gate of the next pixel. The rising edge of ϕV2 also transfers the first line of charge into the horizontal CCD. A second phase transition places the charge packets under the ϕV1 electrode of the next pixel. The sequence completes when ϕV1 is brought low. Clocking of the vertical register in this way is known as accumulation mode clocking. Next, the horizontal CCD reads out the first line of charge using traditional complementary clocking (using ϕH1 and ϕH2 pins) as shown. The falling edge of ϕH2 forces a charge packet over the output gate (OG) onto one of the output nodes (floating diffusion) which controls the output amplifier. The cycle repeats until all lines are read.

1.6 Output Structure

The final gate of the horizontal register is split into two sections, ϕH21 and ϕH22. The split gate structure allows the user to select either of the two output amplifiers. To use the high dynamic range single-stage output (Vout1), tie ϕH22 to a negative voltage to block charge transfer, and tie ϕH21 to ϕH2 to transfer charge. To use the high sensitivity two-stage output (Vout2), tie ϕH21 to a negative voltage and ϕH22 to ϕH2. The charge packets are then dumped onto the appropriate floating diffusion output node whose potential varies linearly with the quantity of charge in each packet. The amount of potential change is determined by the simple expression $\Delta V_{fd}=\Delta Q/C_{fd}$. The translation from electrons to voltages is called the output sensitivity or charge-to-voltage conversion. After the output has been sensed off-chip, the reset clock (ϕR) removes the charge from the floating diffusion via the reset drain (VRD). This, in turn, returns the floating diffusion potential to the reference level determined by the reset drain voltage.

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2.1 Package Configuration

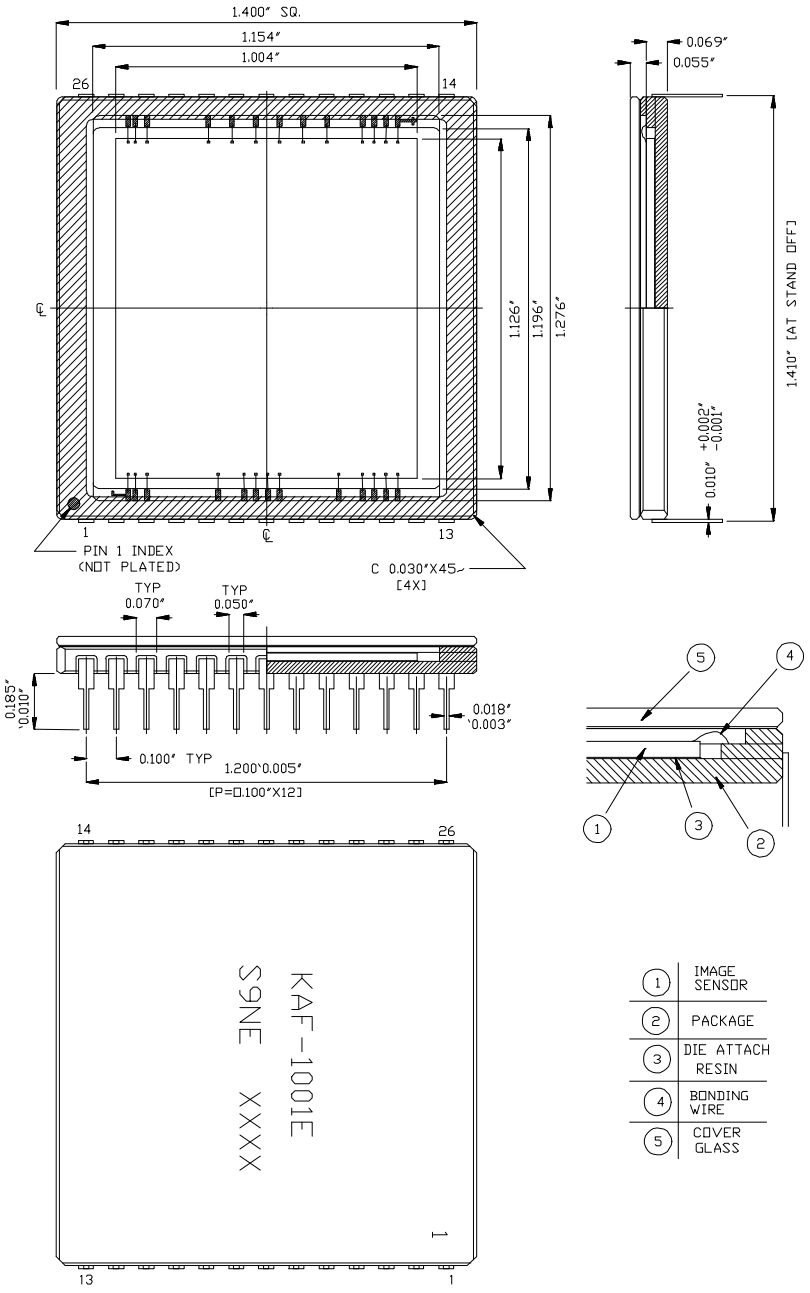

Figure 2 - Package Drawing

2.2 Pin Description

Pin Number	Symbol	Description	Notes
1, 4, 26	SUBSTRATE	Substrate	
2, 21, 25	ϕV2	Vertical (Parallel) CCD Clock - Phase 2	2
3, 22, 24	ϕV1	Vertical (Parallel) CCD Clock - Phase 1	1
5	VOUT2	Video Output from High Sensitivity Two-Stage Amplifier	
6	VDD2	High Sensitivity Two-Stage Amplifier Supply	
7	VLG	First Stage Load Transistor Gate for Two-Stage Amplifier	
8	VSS	Output Amplifier Return	
9	ϕR	Reset Clock	
10	VRD	Reset Drain	
11	VDD1	High Dynamic Range Single-Stage Amplifier Supply	
12	VOUT1	Video Output from High Dynamic Range Single-Stage	
13	OG	Output Gate	
14	ϕH21	Last Horizontal (Serial) CCD Phase - Split Gate	
15	ϕH22	Last Horizontal (Serial) CCD Phase - Split Gate	
16	ϕH1	Horizontal (Serial) CCD Clock - Phase 1	
17	ϕH2	Horizontal (Serial) CCD Clock - Phase 2	
18, 19, 20	N/C	No Connect	
23	GUARD	Guard Ring	

Notes:
1. Pins 3, 22, and 24 must be connected together - only one Phase 1 clock driver is required
2. Pins 2, 21, and 25 must be connected together - only one Phase 2 clock driver is required

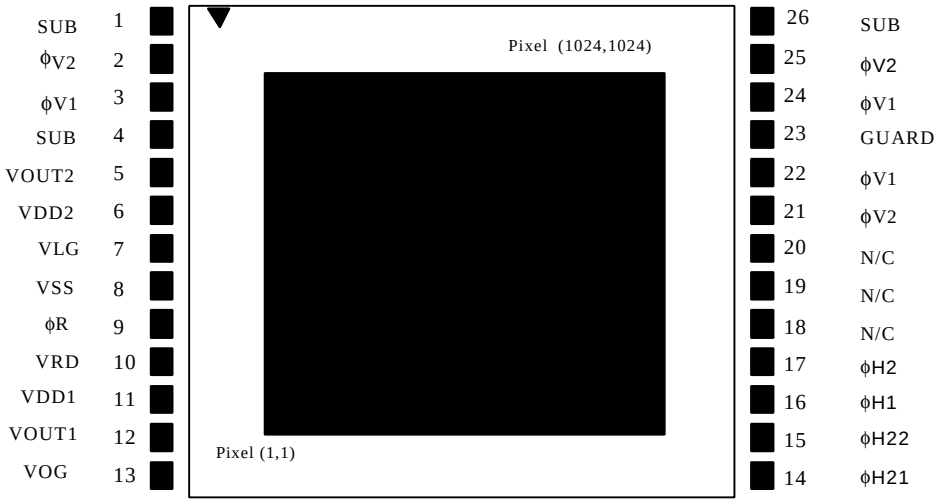

Figure 3 - Pin Identification Diagram

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3.1 Absolute Minimum/Maximum Ratings

		Min.	Max.	Units	Conditions
Temperature	Storage	-100	+80	C	At Device
	Operating	-50	+50		
Voltage	All Clocks	-16	+16	V	VSUB = OV
	OG	0	+8		
	VRD, VSS, VDD, GUARD	0	+20		
Current	Output Bias Current (IDD)		10	mA	
Capacitance	Output Load Capacitance (CLOAD)		10	pF	
Frequency/Time	ϕV1, ϕV2 Pulse Width	8		µs	
	ϕH1, ϕH2		5	MHz	
	ϕR Pulse Width	20		ns	

Warning:
For maximum performance, built-in gate protection has been added only to the OG pin. These devices require extreme care during handling to prevent electrostatic discharge (ESD) induced damage.

3.2 DC Operating Conditions

		Min.	Nom.	Max.	Units	Pin Impedance
VSUB	Substrate	0.0	0.0	0.0	V	Common
VDD	Output Amplifier Supply	15.0	+17.0	17.5	V	5 pf, 2K? (Note 1)
VSS	Output Amplifier Return	1.4	+2.0	2.1	V	5 pf, 2K?
VRD	Reset Drain	11.5	+12	12.5	V	5 pf, 1M?
OG	Output Gate	3.0	+4.0	4.5	V	5 pf, 10M?
GUARD	Guard Ring	7.0	+10.0	15.0	V	350 pF, 10M?
VLG	Load Gate	0.5	+0.0	1.0	V	

Notes:
1. Vdd = 17 volts for aplications where the expected output voltage > 2.0 volts. For applications where the expected useable output voltsge is <2 volts Vdd can be reduced to 15 volts.

3.3 AC Clock Level Conditions

			Min.	Nom.	Max.	Units	Pin Impedance
ϕV1	Vertical Clock - Phase 1	Low	-10.25	-10	-9.8	V	200nF, 10MΩ
		High	0.0	0	1.0	V	
ϕV2	Vertical Clock - Phase 2	Low	-10.25	-10.0	-9.8	V	200nF, 10MΩ
		High	0.0	0	1.0	V	$C\phi_{V1\text{-}V2}$ = 100nF
ϕH1	Horizontal Clock - Phase 1	Low	-2.2	-2.0	-1.8	V	400pF, 10MΩ
		High	7.8	+8.0	8.2	V	
ϕH2	Horizontal Clock - Phase 2	Low	-2.2	-2.0	-1.8	V	250pF, 10MΩ
		High	7.8	+8.0	8.2	V	$C\phi_{h1\text{-}h2}$ =200pF
ϕR	Reset Clock	Low	2.0	3.0	3.5	V	10pF, 10MΩ
		High	9.5	10.0	11.0	V	

			Using the High Gain Output (Vout2)			Using the High Dynamic Range Output (Vout1)				
			Min.	Nom.	Max.	Min.	Nom	Max.	Units	Pin Impedance
ϕH21	Horizontal Clock - Phase 1	Low	-4	ϕH2 low	ϕH2 low		ϕH2		V	10pF, 10MΩ
		High	-4	ϕH2 low	ϕH2 low		ϕH2		V	
ϕH22	Horizontal Clock - Phase 2	Low		ϕH2		-4	ϕH2 low	ϕH2 low	V	10pF, 10MΩ
		High		ϕH2		-4	ϕH2 low	ϕH2 low	V	

Notes:

1. When using Vout1 ϕH21 is clocked identically with ϕH2 while ϕH22 is held at a static level. When using Vout2 ϕH21 and ϕH22 are exchanged so that ϕH22 is identical to ϕH2 and ϕH21 is held at a static level. The static level should be the same voltage as ϕH2 low.
2. The AC and DC operating levels are for room temperature operation. Operation at other temperatures may require adjustments of these voltages. Pins shown with impedances greater than 1 MOhm are expected resistances. These pins are only verified to 1 MOhm.
3. ϕV1, 2 capacitances are accumulated gate oxide capacitance, and so are an over-estimate of the capacitance.
4. This device is suitable for a wide range of applications requiring a variety of different operating conditions. Consult Eastman Kodak in those situations in which operating conditions meet or exceed minimum or maximum levels.

3.4 AC Timing Chart

Description	Symbol	Min.	Nom.	Max.	Units	Notes
ϕH1, ϕH2 Clock Frequency	f_H		4	5	MHz	1, 2, 3
ϕV1, ϕV2 Clock Frequency	f_V		100	125	kHz	1, 2, 3
Pixel Period (1 Count)	t_{pix}	200	250		ns	
ϕH1, ϕH2 Setup Time	$t_{\phi HS}$	500	1000		ns	
ϕV1, ϕV2 Clock Pulse Width	$t_{\phi V}$	4	5		µs	2
Reset Clock Pulse Width	$t_{\phi R}$	20	60		ns	4
Readout Time	$t_{readout}$	226	286		ms	5
Integration Time	t_{int}					6
Line Time	t_{line}	219	277		µs	7

Notes:
1. 50% duty cycle values.
2. CTE may degrade above the nominal frequency.
3. Rise and fall times (10/90% levels) should be limited to 5-10% of clock period. Crossover of register clocks should be between 40-60% of amplitude.
4. ϕR should be clocked continuously
5. $t_{readout} = (1032 * t_{line})$
6. Integration time (t_{int}) is user specified. Longer integration times will degrade noise performance due to dark signal fixed pattern and shot noise.
7. $t_{line} = (3 * t_{\phi V}) + t_{\phi HS} + 1044 * t_{pix} + t_{pix}$

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AC Timing Diagram

Note: This device is suitable for a wide range of applications requiring a variety of different timing frequencies. Therefore, only maximum and minimum values are shown above. Consult Eastman Kodak in those situations that require special consideration

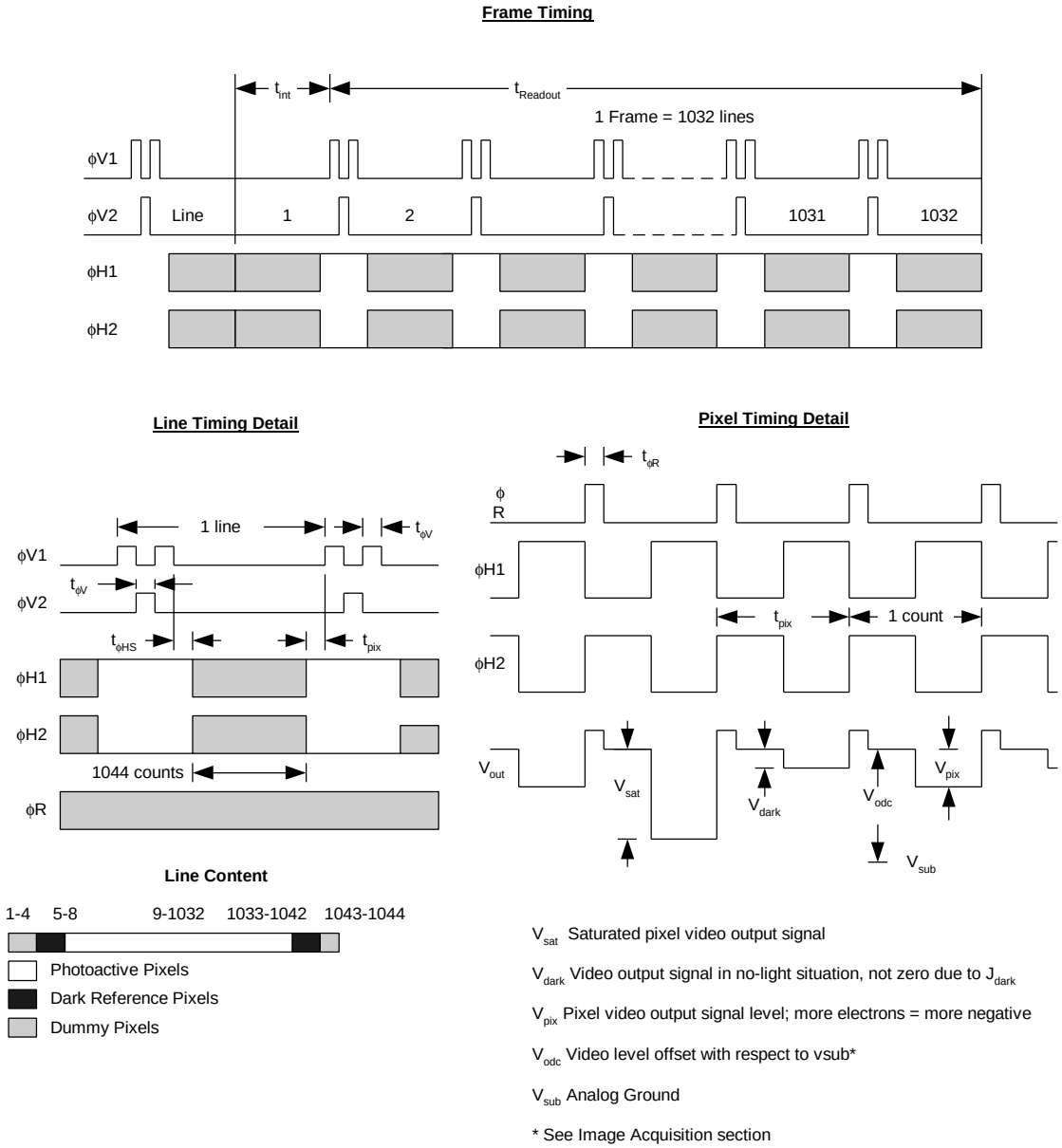

Figure 4 - Timing Diagram

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4.1 Image Specifications

All values derived using nominal operating conditions with the recommended timing. Correlated doubling sampling of the output is assumed and recommended. Many units are expressed in electrons - to convert to voltage, multiply by the amplifier sensitivity.

Electro-Optical

Symbol	Parameter	Min.	Nom.	Max.	Units	Condition
F F	Optical Fill Factor		100		%	
PRNU	Photoresponse Non-uniformity			5	% rms	Full Array
QE	Quantum Efficiency (450, 550, 650nm)					See QE curve

CCD Parameters Common To both Outputs

Symbol	Parameter	Min.	Nom.	Max.	Units	Condition
N_{e^-sat}	Sat. Signal - Vccd register	550	650		ke	Note 2
J_d	Dark Current		15.3 550	30 1080	pA/cm^2 e^-pixel/sec	25°C (mean of all pixels)
DCDR	Dark Current Doubling Temp	5	6	7	^oC	
DSNU	Dark Signal Non-uniformity			1080	e-/pix/sec	Note 4
CTE	Charge Transfer Efficiency		.99997			Note 5
t_{VH}	V-H CCD Transfer Time		32		µs	Notes 6, 7
Bs	Blooming Suppression		none			

CCD Parameters Specific to High Gain Output Amplifier

Symbol	Parameter	Min.	Nom.	Max.	Units	Condition
Vout/Ne-	Output Sensitivity	9	11		uV/electron	
N_{e^-sat}	Sat. Signal	180	200	240	ke^-	Note 1
n_{e^-total}	Total Sensor Noise		13	20	e^- rms	Note 8
F_H	Horizontal CCD Frequency:		2	5	MHz	Note 6
DR	Dynamic Range :	79	83		dB	Note 9

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CCD Parameters Specific to Low Gain (high dynamic range) Output Amplifier

Symbol	Parameter	Min.	Nom.	Max	Units	Condition
Vout/Ne-	Output Sensitivity	1.7	2		uV/electron	
N_{e^-sat}	Sat. Signal	1400	1500	1800	ke^-	Note 3
n_{e^-total}	Total Sensor Noise		22	30	e^- rms	Note 8
F_H	Horizontal CCD Frequency:		0.5	2	MHz	Note 6
DR	Dynamic Range :	89	87		dB	Note 9

Notes:
1. Point where the output saturates when operated with nominal voltages.
2. Signal level at the onset of blooming in the vertical (parallel) CCD register
3. Maximum signal level at the output of the high dynamic range output. This signal level will only be achieved when binning pixels containing large signals.
4. None of 64 sub arrays (128 x 128) exceed the maximum dark current specification.
5. For 2MHz data rate and T = 30 C to -40°C.
6. Using maximum CCD frequency and/or minimum CCD transfer times may compromise performance
7. Time between the rising edge of $\phi V1$ and the first falling edge of $\phi H1$
8. At $T_{integration}$ = 0; data rate = 1 MHz; temperature = -30 C
9. Uses 20LOG($N_{e^- sat}$ / $n_{e^- total}$) where $N_{e^- sat}$ refers to the appropriate saturation signal.

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4.2 Cosmetic Grades

Standard:

Class	Point Defects	Cluster Defects	Column Defects
C1	20	2	0
C2	40	10	0
C3	80	20	10

UV Enhanced:

U2	40	10	0	Note 1

Notes:
1. Sensors with an UV enhancement coating are available with the same cosmetic grade as the uncoated C2.

Dark Defect — A pixel which deviates by more than 20% from neighboring pixels when illuminated to 70% of saturation

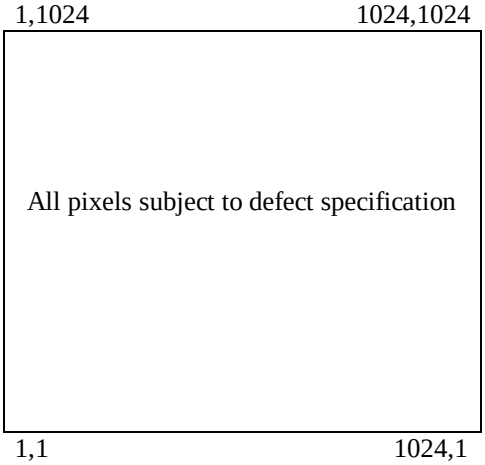
Bright Defect — A pixel whose dark current exceeds 4500 electrons/pixel/second at 25°C

Cluster Defect — A grouping of not more than 5 adjacent point defects.

Column Defect
1) A grouping point defects along a single column. (Dark Column)
2) A column that contains a pixel whose dark current exceeds 150,000 electrons/pixel/second at 25 C. (Bright Column)
3) A column that does not exhibit the minimum charge capacity specification. (Low charge capacity)
4) A column that loses >500 electrons when the array is illuminated to a signal level of 2000 electrons/pix. (Trap like defects)

Neighboring Pixels — The surrounding 128 x 128 pixels of ± 64 columns/rows

Defects are separated by no less than 3 pixels in any one direction.



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4.3 Typical Performance Data

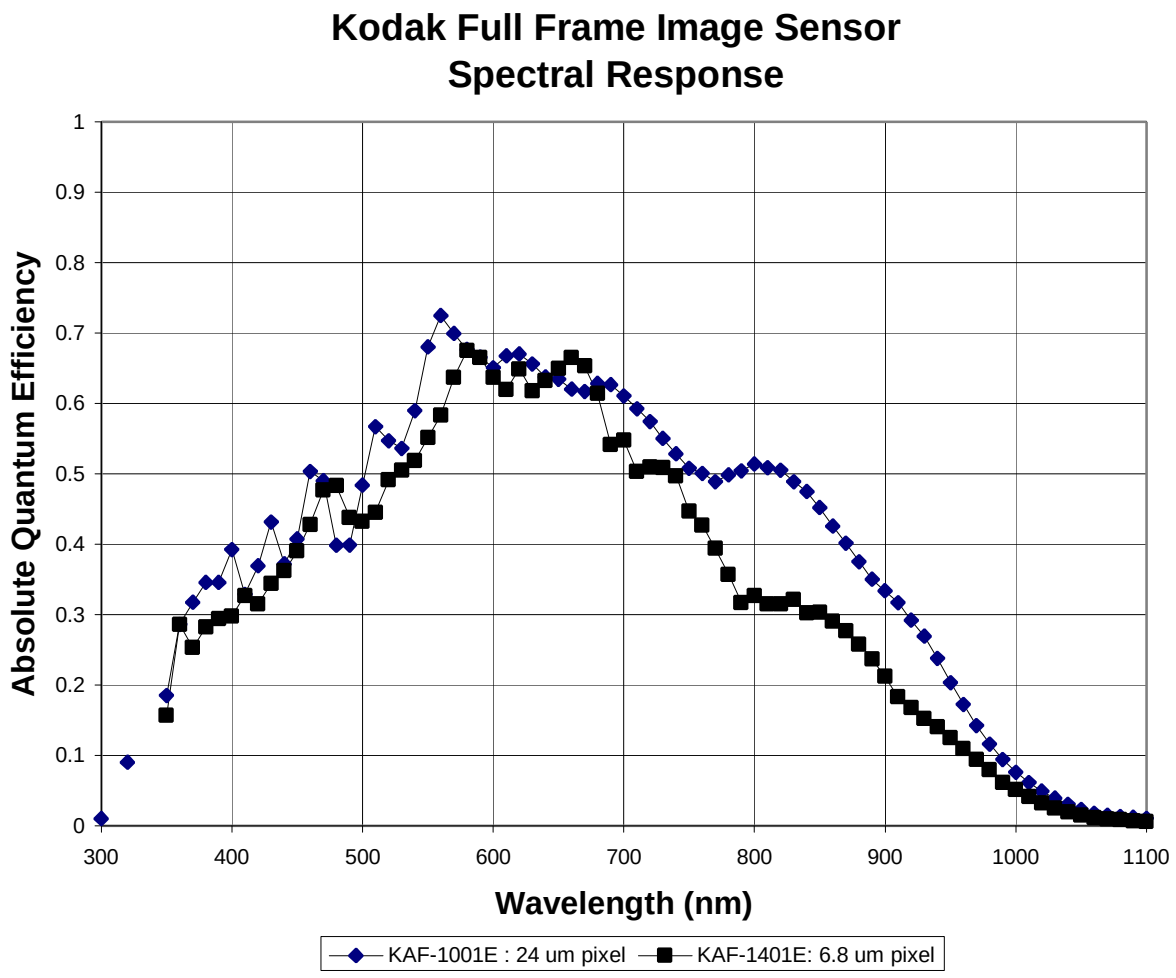

Figure 5 - Typical Spectral Response

Figure 5 shows a representative spectral response of front side illuminated transparent gate full frame image sensors. The KAF-1001E with 24µm pixels has higher response than the 6.8µm pixel sensor at wavelengths greater than 750nm because it is constructed on a lower resistivity silicon substrate. The resulting collection volume of each pixel more efficiently collects signal generated deeper within the silicon.

Most of the two phase CCD pixels are designed so that each of the electrodes occupies half of the pixel area. The KAF-1001E was not designed this way but instead is designed with the transparent electrode occupying greater than half the pixel area. This further improves the benefits of the transparent gate.

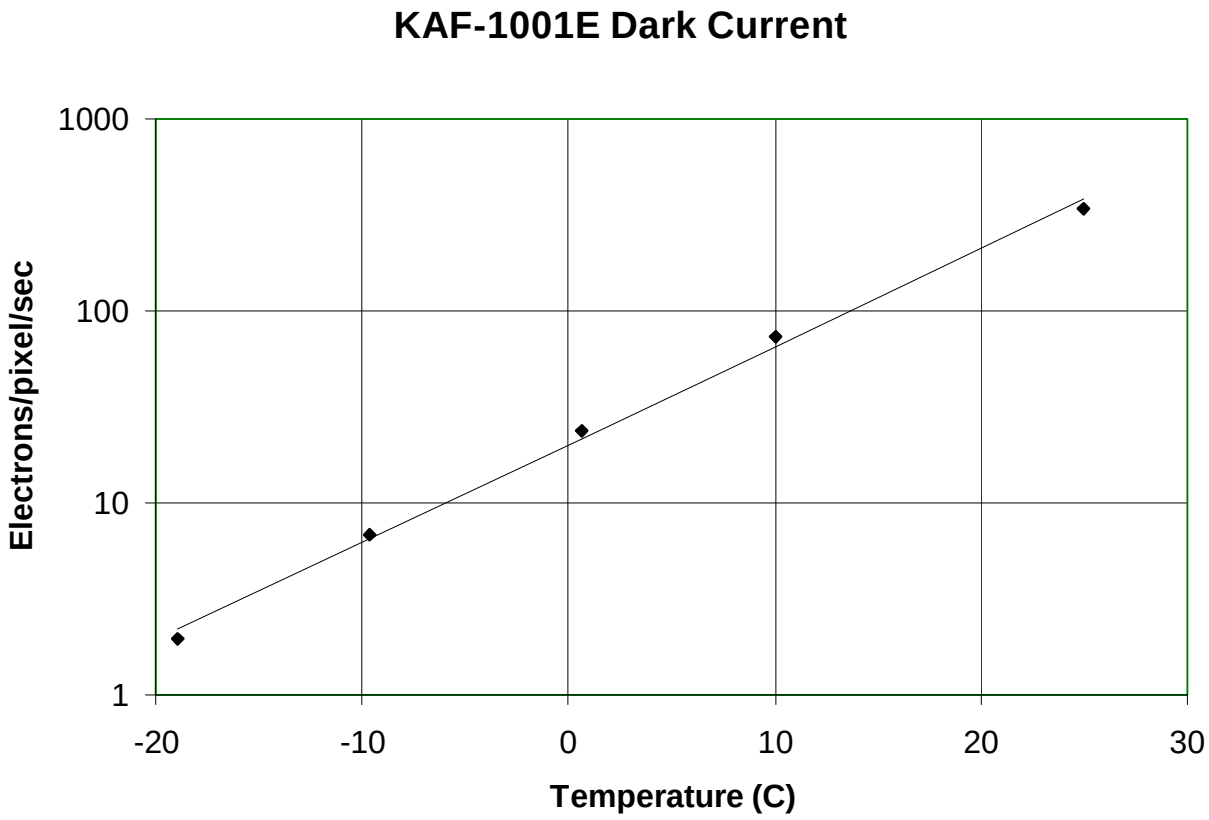

Figure 6 - Dark Current as a Function of Temperature

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5.1 Quality Assurance and Reliability

5.1.1 Quality Strategy: All devices will conform to the specifications stated in this document. This is accomplished through a combination of statistical process control and inspection at key points of the production process.

5.1.2 Replacement: All devices are warranted against failure in accordance with the terms of Terms of Sale.

5.1.3 Cleanliness: Devices are shipped free of contamination, scratches, etc. that would cause a visible defect.

5.1.4 ESD Precautions: Devices are shipped in a static-safe container and should only be handled at static-safe workstations.

5.1.5 Reliability: Information concerning the quality assurance and reliability testing procedures and results are available from the Microelectronics Technology Division and can be supplied upon request.

5.1.6 Test Data Retention: Devices have an identifying number of traceable to a test data file. Test data is kept for a period of 2 years after date of shipment.

5.2 Ordering Information

Address all inquiries and purchase orders to:

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Kodak reserves the right to change any information contained herein without notice. All information furnished by Kodak is believed to be accurate.

APPENDIX

Appendix 1 – Part Number Availability

Device	Part Number	Features
KAF-1001E	2H4489	Clear Sealed Cover Glass, Class 1
KAF-1001E	2H4490	Clear Sealed Cover Glass, Class 2
KAF-1001E	2H4492	Clear Sealed Cover Glass, Engineering Grade
KAF-1001E	2H4493	Clear Sealed Cover Glass, Mechanical Grade
KAF-1001E	2H4483	Temporary Cover, Class 1
KAF-1001E	2H4484	Temporary Cover, Class 2
KAF-1001E	2H4486	Temporary Cover, Engineering Grade
KAF-1001E	2H4487	Temporary Cover, Mechanical Grade
KAF-1001EU	2H4692	Lumogen enhanced, Quartz Sealed Cover Glass, Class 2
KAF-1001EU	2H4693	Lumogen enhanced, Temporary Cover, Class 2