KAF - 0261E

512(H) x 512(V) Pixel

Enhanced Response

Full-Frame CCD Image Sensor

Performance Specification

Eastman Kodak Company

Image Sensor Solutions

Rochester, New York 14650

Revision 1

January 3, 2000

Eastman Kodak Company – Image Sensor Solutions - Rochester, NY 14650-2010
Phone (716) 722-4385 Fax (716) 477-4947
Web: www.kodak.com/go/ccd E-mail: ccd@kodak.com

TABLE OF CONTENTS

APPENDIX

FIGURES

Eastman Kodak Company – Image Sensor Solutions - Rochester, NY 14650-2010
Phone (716) 722-4385 Fax (716) 477-4947
Web: www.kodak.com/go/ccd E-mail: ccd@kodak.com

1.1 Features

- **Front Illuminated Full-Frame Architecture**
- **512(H) x 512(V) Photosensitive Pixels**
- **Transparent Gate True Two Phase Technology (Enhanced Spectral Response)**
- **20µm(H) x 20µm(V) Pixel Size**
- **1:1 Aspect Ratio**
- **100% Fill Factor**
- **Single Readout Register**
- **2 Clock Selectable Outputs**
  - **High Gain Output (10 µV/e^-) for low noise**
  - **Low Gain Output (3.5 µV/e^-) for high dynamic range**
- **Low Dark Current (<30pA/cm^2 @ T=25^{o}C)**

1.2 Description

The KAF-0261E is a high performance, silicon charge-coupled device (CCD) designed for a wide range of image sensing applications in the 0.3µm to 1.1µm wavelength band. Common applications include medical, scientific, military, machine and industrial vision.

The sensor is built with a true two-phase CCD technology employing a transparent gate. This technology simplifies the support circuits that drive the sensor and reduces the dark current without compromising charge capacity. The transparent gate results in spectral response increased ten times at 400nm, compared to a front side illuminated standard polysilicon gate technology. The sensitivity is increased 50% over the rest of the visible wavelengths.

The low dark current of the KAF-0261E makes this device suitable for low light imaging applications without sacrificing in charge capacity. The clock selectable on-chip output amplifiers have been specially designed to meet two different needs. The first is a high sensitivity 2-stage output with 10µV/e^- charge to voltage conversion ratio. The second is a single stage output with 3.5µV/e^- charge to voltage conversion ratio.

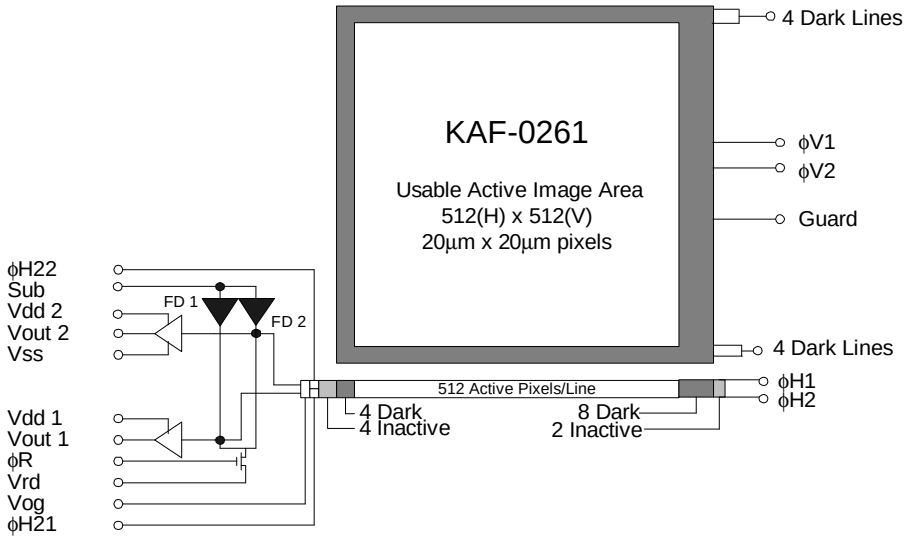


Figure 1 - Functional Block Diagram

Shaded areas represent 4 non-imaging pixels at the beginning and 8 non-imaging pixels at the end of each line.
There are also 4 non-imaging lines at the top and bottom of each frame.

Eastman Kodak Company – Image Sensor Solutions - Rochester, NY 14650-2010
Phone (716) 722-4385 Fax (716) 477-4947
Web: www.kodak.com/go/ccd E-mail: ccd@kodak.com

1.3 Architecture

The KAF-0261E consists of one vertical (parallel) CCD shift register, one horizontal (serial) CCD shift register and a selectable high or low gain output amplifier. (See Figure 1.) Both registers incorporate two-phase buried channel CCD technology. The vertical register consists of 20µm x 20µm photocapacitor sensing elements (pixels) which also serves as the transport mechanism. The pixels are arranged in a 512(H) x 512(V) array; an additional 12 columns (4 at the left and 8 at the right) and 8 rows (4 each at top and bottom) of non-imaging pixels are added as dark reference. Because there is no storage array, this device must be synchronized with strobe illumination or shuttered during readout.

1.4 Image Acquisition

An image is acquired when incident light, in the form of photons, falls on the array of pixels in the vertical CCD register and creates electron-hole pairs (or simply electrons) within the silicon substrate. This charge is collected locally by the formation of potential wells created at each pixel site by induced voltages on the vertical register clock lines (ϕV1, ϕV2). These same clock lines are used to implement the transport mechanism as well. The amount of charge collected at each pixel is linearly dependent on light level and exposure time and non-linearly dependent on wavelength until the potential well capacity is exceeded. At this point charge will 'bloom' into vertically adjacent pixels.

1.5 Charge Transport

Integrated charge is transported to the output in a two step process. Rows of charge are first shifted line by line into the horizontal CCD. 'Lines' of charge are then shifted to the output pixel by pixel. Referring to the timing diagram illustration in section 2.7, integration of charge is performed with ϕV1 and ϕV2 held low. Transfer to horizontal CCD begins when ϕV1 is brought high causing charge from the ϕV1 and ϕV2 gates to combine under the ϕV1 gate. ϕV1 and ϕV2 now reverse their polarity causing the charge packets to 'spill' forward under the ϕV2 gate of the next pixel. The rising edge of ϕV2 also transfers the first line of charge into the horizontal CCD. A second phase transition places the charge packets under the ϕV1 electrode of the next pixel.

The sequence completes when ϕV1 is brought low. Clocking of the vertical register in this way is known as accumulation mode clocking. Next, the horizontal CCD reads out the first line of charge using traditional complementary clocking (using ϕH1 and ϕH2 pins) as shown. The falling edge of ϕH2 forces a charge packet over the output gate (OG) onto one of the output nodes (floating diffusion) which is buffered by the output amplifier. The cycle repeats until all lines are read.

1.6 Output Structure

The final gate of the horizontal register is split into two sections, ϕH21 and ϕH22. The split gate structure allows the user to select either of the two output amplifiers. To use the high dynamic range single-stage output (Vout1), tie ϕH22 to a negative voltage to block charge transfer, and tie ϕH21 to ϕH2 to transfer charge. To use the high sensitivity two-stage output (Vout2), tie ϕH21 to a negative voltage and ϕH22 to ϕH2. The charge packets are then dumped onto the appropriate floating diffusion output node whose potential varies linearly with the quantity of charge in each packet. The amount of potential change is determined by the simple expression $\Delta V_{fd}=\Delta Q/C_{fd}$.

The translation from electrons to voltages is called the output sensitivity or charge-to-voltage conversion. After the output has been sensed off-chip, the reset clock (ϕR) removes the charge from the floating diffusion via the reset drain (VRD). This, in turn, returns the floating diffusion potential to the reference level determined by the reset drain voltage.

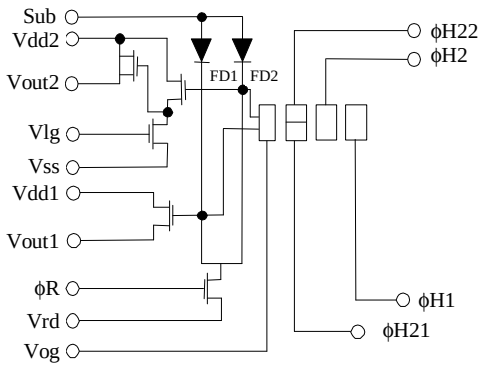


Figure 2 - Output Structure

Eastman Kodak Company – Image Sensor Solutions - Rochester, NY 14650-2010
Phone (716) 722-4385 Fax (716) 477-4947
Web: www.kodak.com/go/ccd E-mail: ccd@kodak.com

2.1 Package Diagram

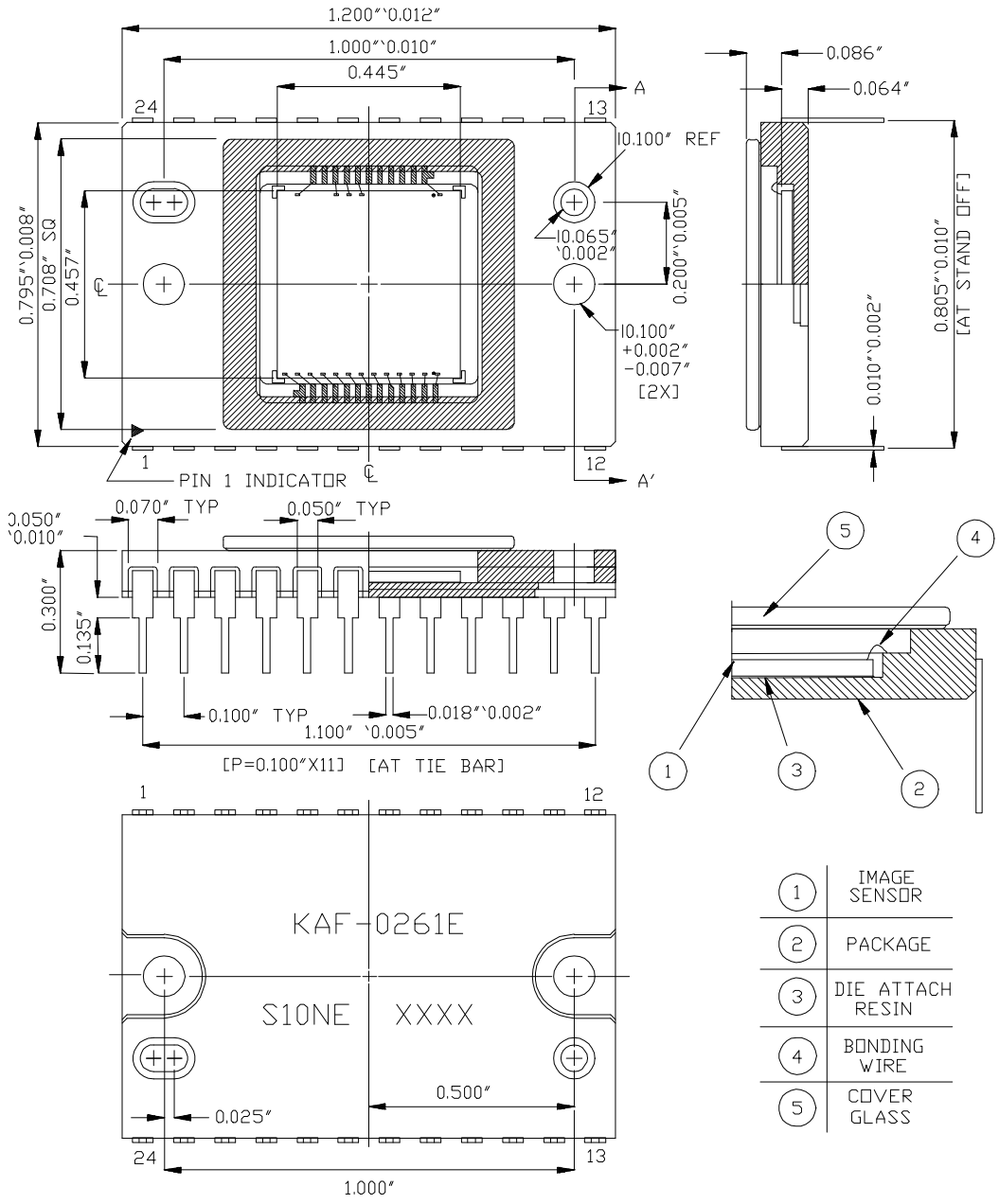


Figure 3 - Package Configuration

Eastman Kodak Company – Image Sensor Solutions - Rochester, NY 14650-2010
Phone (716) 722-4385 Fax (716) 477-4947
Web: www.kodak.com/go/ccd E-mail: ccd@kodak.com

2.2 Pin Description

PIN No.	SYMBOL	DESCRIPTION	NOTES
1	OG	Output Gate	
2	VOUT2	Video Output from High Sensitivity Two-Stage	
3	VDD1/VD	Amplifier Supply for VOUT1 and VOUT2 amplifiers	
4	VRD	Reset Drain	
5	ϕR	Reset Clock	
6	VSS	Output Amplifier Return	
7	ϕH1	Horizontal (Serial) CCD Clock - Phase 1	
8	ϕH2	Horizontal (Serial) CCD Clock - Phase 2	
9	VOUT1	Video Output from High Dynamic Range Single-Stage	
10	ϕH21	Last Horizontal (Serial) CCD Phase - Split Gate	
11	ϕH22	Last Horizontal (Serial) CCD Phase - Split Gate	
12	N/C	No Connect	
13, 14	SUBSTRA	Substrate	
15, 16, 21, 22	ϕV1	Vertical (Parallel) CCD Clock - Phase 1	1
17, 18, 19, 20	ϕV2	Vertical (Parallel) CCD Clock - Phase 2	2
23	GUARD	Guard Ring	
24	VLG	First Stage Load Transistor Gate for Two-Stage	

Notes:
1. Pins 15, 16, 21, and 22 must be connected together - only one Phase 1-clock driver is required
2. Pins 17, 18, 19, and 20 must be connected together - only one Phase 2-clock driver is required

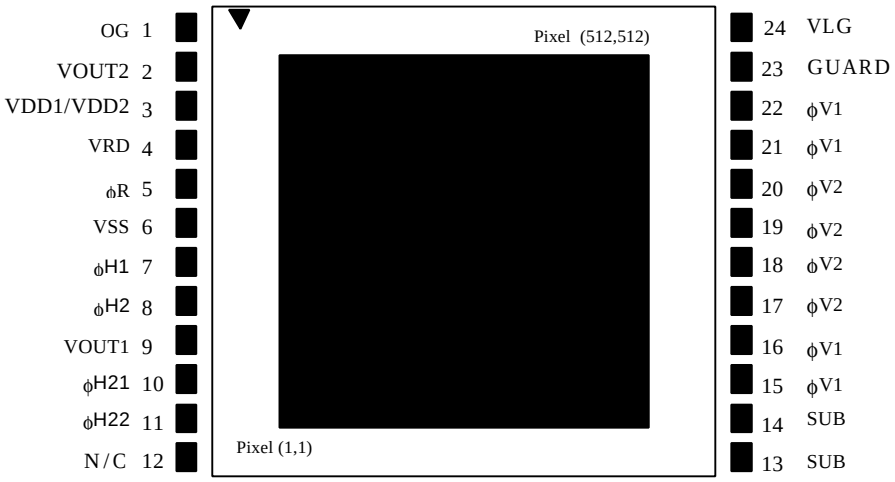


Figure 4 - Pinout Diagram

Eastman Kodak Company – Image Sensor Solutions - Rochester, NY 14650-2010
Phone (716) 722-4385 Fax (716) 477-4947
Web: www.kodak.com/go/ccd E-mail: ccd@kodak.com

2.3 Absolute Minimum/Maximum Ratings

		Min.	Max.	Units	Conditions
Temperature	Storage	-100	+80	C	At Device
	Operating	-70	+50	C	
	All Clocks	-16	+16	V	Note 1
Voltage	OG	0	+8	V	Note 2
	VRD, VSS, VDD, GUARD	0	+20	V	Note 2
Current	Output Bias Current (IDD)		10	mA	
Capacitance			10	pF	

Notes:
1. Voltage between any two clocks or between any clock and Vsub.
   Warning:
   For maximum performance, built-in gate protection has been added only to the OG pin. These devices require extreme care during handling to prevent electrostatic discharge (ESD) induced damage.
2. Voltage with respect to Vsub.

2.4 DC Operating Conditions

		Min.	Nom.	Max.	Units	Pin Impedance
VSUB	Substrate	0.0	0.0	0.0	V	Common
VDD	Output Amplifier Supply	15.0	+17.0	17.5	V	5 pf, 2KΩ (Note 1)
VSS	Output Amplifier Return	1.4	+2.0	2.1	V	5 pf, 2KΩ
VRD	Reset Drain	11.5	+12	12.5	V	5 pf, 1MΩ
OG	Output Gate	3.0	+4.0	4.5	V	5 pf, 10MΩ
GUARD	Guard Ring	9.0	+10.0	15.0	V	350 pF, 10MΩ
VLG	Load Gate	VSS - 1.0	VSS	VSS + 1.0	V	

Notes
1. Vdd = 17 volts for applications where the expected output voltage > 2.0 volts. For applications where the expected useable output voltage is < 2 volts Vdd can be reduced to 15 volts.

2.5 AC Clock Level Conditions

			Min.	Nom.	Max.	Units	Pin Impedance
ϕV1	Vertical Clock - Phase 1	Low	-10.2	-10.0	-9.0	V	13 nf, 10MΩ
		High	0.0	0	2.0	V	
ϕV2	Vertical Clock - Phase 2	Low	-10.2	-10.0	-9.0	V	16 nf, 10MΩ
		High	0.0	0	2.0	V	
ϕH1	Horizontal Clock - Phase 1	Low	-2.2	-2.0	-1.8	V	160 pf, 10MΩ
		High	7.8	+8.0	8.2	V	
ϕH2	Horizontal Clock - Phase 2	Low	-2.2	-2.0	-1.8	V	110 pf, 10MΩ
		High	7.8	+8.0	8.2	V	$C\emptyset_{h1\text{-}h2}$ = 75pf
ϕR	Reset Clock	Low	2.0	3.0	3.5	V	10 pF, 10MΩ
		High		10.0		V	

			Using the High Gain Output (Vout 2)			Using the High Dynamic Range Output (Vout1)				
			Min.	Nom.	Max.	Min.	Nom.	Max.	Units	Pin Impedance
ϕH21	Horizontal Clock - Phase 1	Low	-4	ϕH2 low	ϕH2 low		ϕH2		V	10 pF, 10MΩ
		High	-4	ϕH2 low	ϕH2 low		ϕH2		V	
ϕH22	Horizontal Clock - Phase 2	Low		ϕH2		-4	ϕH2 low	ϕH2 low	V	10 pF, 10MΩ
		High		ϕH2		-4	ϕH2 low	ϕH2 low	V	

Note: When using Vout1 ϕH21 is clocked identically with ϕH2 while ϕH22 is held at a static level. When using Vout2 ϕH21 and ϕH22 are exchanged so that ϕH22 is identical to ϕH2 and ϕH21 is held at a static level. The static level should be the same voltage as ϕH2 low.

Note: The AC and DC operating levels are for room temperature operation. Operation at other temperatures may require adjustments of these voltages. Pins shown with impedances greater than 1 MOhm are expected resistances. These pins are only verified to 1 MOhm.

Note: ØV1, 2 capacitances are accumulated gate oxide capacitance, and so are an over-estimate of the capacitance.

Note: This device is suitable for a wide range of applications requiring a variety of different operating conditions. Consult Eastman Kodak in those situations in which operating conditions meet or exceed minimum or maximum levels.

Eastman Kodak Company – Image Sensor Solutions - Rochester, NY 14650-2010
Phone (716) 722-4385 Fax (716) 477-4947
Web: www.kodak.com/go/ccd E-mail: ccd@kodak.com

2.6 AC Timing Chart

Description	Symbol	Min.	Nom.	Max.	Units	Notes
ϕH1, ϕH2 Clock Frequency	f_H		5	8	MH	1, 2, 3
V1, V2 Clock Frequency	f_V		100	125	KH	1, 2, 3
Pixel Period (1 Count)	tpix	125	200		ns	
ϕH1, ϕH2 Set-up Time	$t_{\phi HS}$	500	100		ns	
ϕV1, ϕV2 Clock Pulse Width	$t_{\phi V}$	4	5		µs	2
Reset Clock Pulse Width	$t_{\phi R}$	10	20		ns	4
Readout Time	$t_{readout}$	40	64		ms	5
Integration Time	t_{int}					6
Line Time	t_{line}	78	122		µs	7

Notes:
1. 50% duty cycle values.
2. CTE may degrade above the nominal frequency.
3. Rise and fall times (10/90% levels) should be limited to 5-10% of clock period. Crossover of register clocks should be between 40-60% of amplitude.
4. ϕR should be clocked continuously
5. $t_{readout} = (520 * t_{line})$
6. Integration time (t_{int}) is user specified. Longer integration times will degrade noise performance due to dark signal fixed pattern and shot noise.
7. $t_{line} = (3 * t_{\phi V}) + t_{\phi HS} + 530 * t_{pix} + t_{pix}$

Eastman Kodak Company – Image Sensor Solutions - Rochester, NY 14650-2010
Phone (716) 722-4385 Fax (716) 477-4947
Web: www.kodak.com/go/ccd E-mail: ccd@kodak.com

2.7 AC Timing Diagram

Note: This device is suitable for a wide range of applications requiring a variety of different timing frequencies. Therefore, only maximum and minimum values are shown above. Consult Eastman Kodak in those situations, which require special consideration

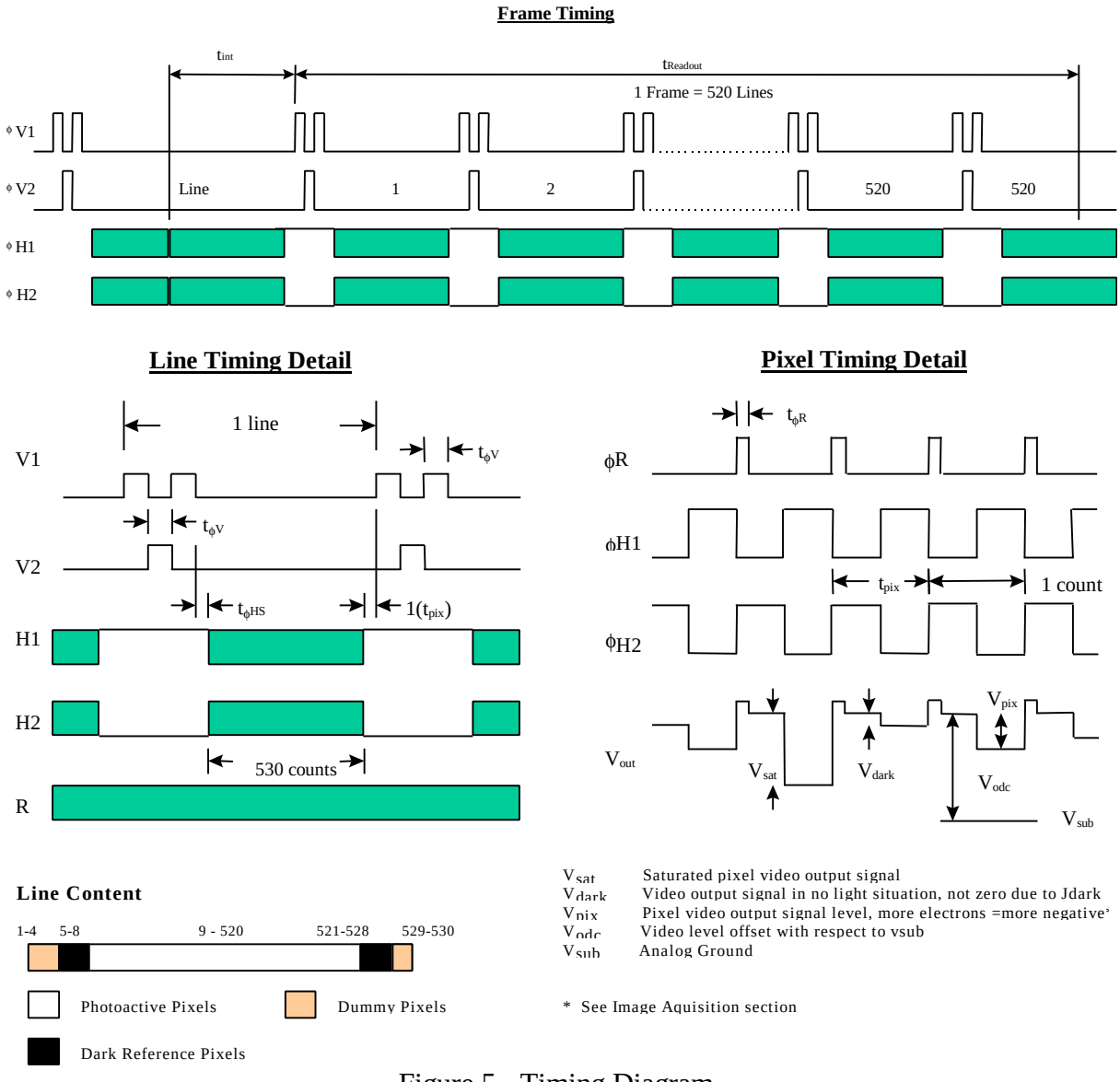


Figure 5 - Timing Diagram

Eastman Kodak Company – Image Sensor Solutions - Rochester, NY 14650-2010
Phone (716) 722-4385 Fax (716) 477-4947
Web: www.kodak.com/go/ccd E-mail: ccd@kodak.com

3.1 Image Specifications

All values derived using nominal operating conditions with the recommended timing. Correlated doubling sampling of the output is assumed and recommended. Many units are expressed in electrons - to convert to voltage, multiply by the amplifier sensitivity.

Electro-Optical

Symbol	Parameter	Min.	Nom.	Max.	Units	Condition
F F	Optical Fill Factor		100		%	
PRNU	Photoresponse Non-uniformity			5	% rms	Full Array
QE	Quantum Efficiency (450, 550, 650 nm)					See Q.E. curve (Figure 6.)

CCD Parameters Common To Both Outputs

Symbol	Parameter	Min	Nom.	Max.	Units	Condition
N_{e^-sat}	Sat. Signal - Vccd register	450	500		ke^-	Note 2
J_d	Dark Current		15.3 400	30 750	pA/cm^2 e^-pixel/sec	25 C (mean of all pixels)
DCDR	Dark Current Doubling Temp	5	6.3	7.5	^oC	
DSNU	Dark Signal Non-uniformity			750	e-/pix/sec	Note 4
CTE	Charge Transfer Efficiency		.99997			Note 5
PRNL	Photoresponse Non-Linearity		1	2	%	Note 9
Bs	Blooming Suppression		none			

CCD Parameters Specific to High Gain Output Amplifier

Symbol	Parameter	Min	Nom	Max	Unit	Condition
Vout/Ne-	Output Sensitivity	9	10		uV/electron	
N_{e^-sat}	Sat. Signal	180	200	240	ke^-	Note 1
N_{e^-total}	Total Sensor Noise:		13	20	e^- rms	Note 7
F_H	Horizontal CCD Frequency:		2	5	MHz	Note 6
DR	Dynamic Range:	79	83		dB	Note 8

Eastman Kodak Company – Image Sensor Solutions - Rochester, NY 14650-2010
Phone (716) 722-4385 Fax (716) 477-4947
Web: www.kodak.com/go/ccd E-mail: ccd@kodak.com

CCD Parameters Specific to Low Gain (high dynamic range) Output Amplifier

Symbol	Parameter	Min.	Nom.	Max.	Units	Condition
Vout/Ne-	Output Sensitivity	3.2	3.5		uV/electron	
N_{e^-sat}	Sat. Signal	550K	628K		ke^-	Note 3
N_{e^-total}	Total Sensor Noise:		22	30	e^- rms	Note 7
F_H	Horizontal CCD Frequency:		0.5	2	MHz	Note 6
DR	Dynamic Range:	89	87		dB	Note 8

Notes:
1. Point where the output saturates when operated with nominal voltages.
2. Signal level at the onset of blooming in the vertical (parallel) CCD register
3. Maximum signal level at the output of the high dynamic range output. This signal level will only be achieved when binning pixels containing large signals.
4. None of 16 sub arrays (128 x 128) exceed the maximum dark current specification.
5. For 2MHz data rate and T = 30 C to -40 C.
6. Using maximum CCD frequency and/or minimum CCD transfer times may compromise performance
7. At $T_{integration}$ = 0; data rate = 1 MHz; temperature = -30 C
8. Uses 20LOG($N_{e^- sat}$ / $n_{e^- total}$) where $N_{e^- sat}$ refers to the appropriate saturation signal.
9. Worst case deviation from straight line fit, between 1% and 90% of Vsat.

Eastman Kodak Company – Image Sensor Solutions - Rochester, NY 14650-2010
Phone (716) 722-4385 Fax (716) 477-4947
Web: www.kodak.com/go/ccd E-mail: ccd@kodak.com

3.2 Cosmetic Specification

Standard:

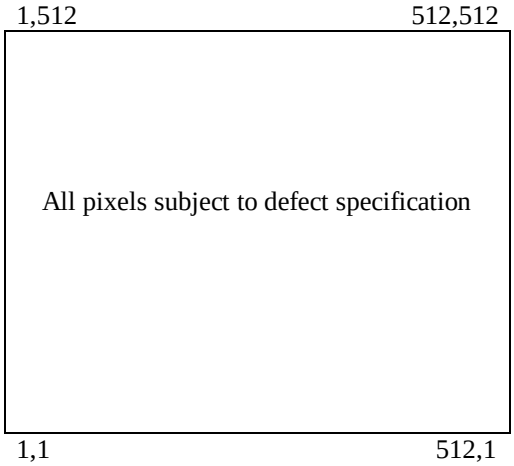
Class	Point Defects	Cluster Defects	Column Defects
C0	0	0	0
C1	10	4	0

UV Enhanced:

UV	10	4	0

Dark Defect	A pixel which deviates by more than 20% from neighboring pixels when illuminated to 70% of saturation
Bright Defect	A pixel whose dark current exceeds 4500 electrons/pixel/second at 25°C
Cluster Defect	A grouping of not more than 5 adjacent point defects.
Column Defect	1) A grouping point defects along a single column. (Dark Column) 2) A column that contains a pixel whose dark current exceeds 150,000 electrons/pixel/second at 25 C. (Bright Column) 3) A column that does not exhibit the minimum charge capacity specification. (Low charge capacity) 4) A column that loses >500 electrons when the array is illuminated to a signal level of 2000 electrons/pix. (Trap like defects)
Neighboring Pixels	The surrounding 128 x 128 pixels of ± 64 columns/rows

Defects are separated by no less than 3 pixels in any one direction.



Eastman Kodak Company – Image Sensor Solutions - Rochester, NY 14650-2010
Phone (716) 722-4385 Fax (716) 477-4947
Web: www.kodak.com/go/ccd E-mail: ccd@kodak.com

4.1 Quality Assurance and Reliability

4.1.1 Quality Strategy: All devices will conform to the specifications stated in this document. This is accomplished through a combination of statistical process control and inspection at key points of the production process.

4.1.2 Replacement: All devices are warranted against failure in accordance with the terms of Terms of Sale.

4.1.3 Cleanliness: Devices are shipped free of contamination, scratches, etc. that would cause a visible defect.

4.1.4 ESD Precautions: Devices are shipped in a static-safe container and should only be handled at static-safe workstations.

4.1.5 Reliability: Information concerning the quality assurance and reliability testing procedures and results are available from the Image Sensor Solutions and can be supplied upon request.

4.1.6 Test Data Retention: Devices have an identifying number of traceable to a test data file. Test data is kept for a period of 2 years after date of shipment.

4.2 Ordering Information

Address all inquiries and purchase orders to:

Image Sensor Solutions
Eastman Kodak Company
Rochester, New York 14650-2010
Phone: (716) 722-4385
Fax: (716) 477-4947
E-Mail: ccd@kodak.com

Kodak reserves the right to change any information contained herein without notice. All information furnished by Kodak is believed to be accurate.

5.1 Typical Performance Data

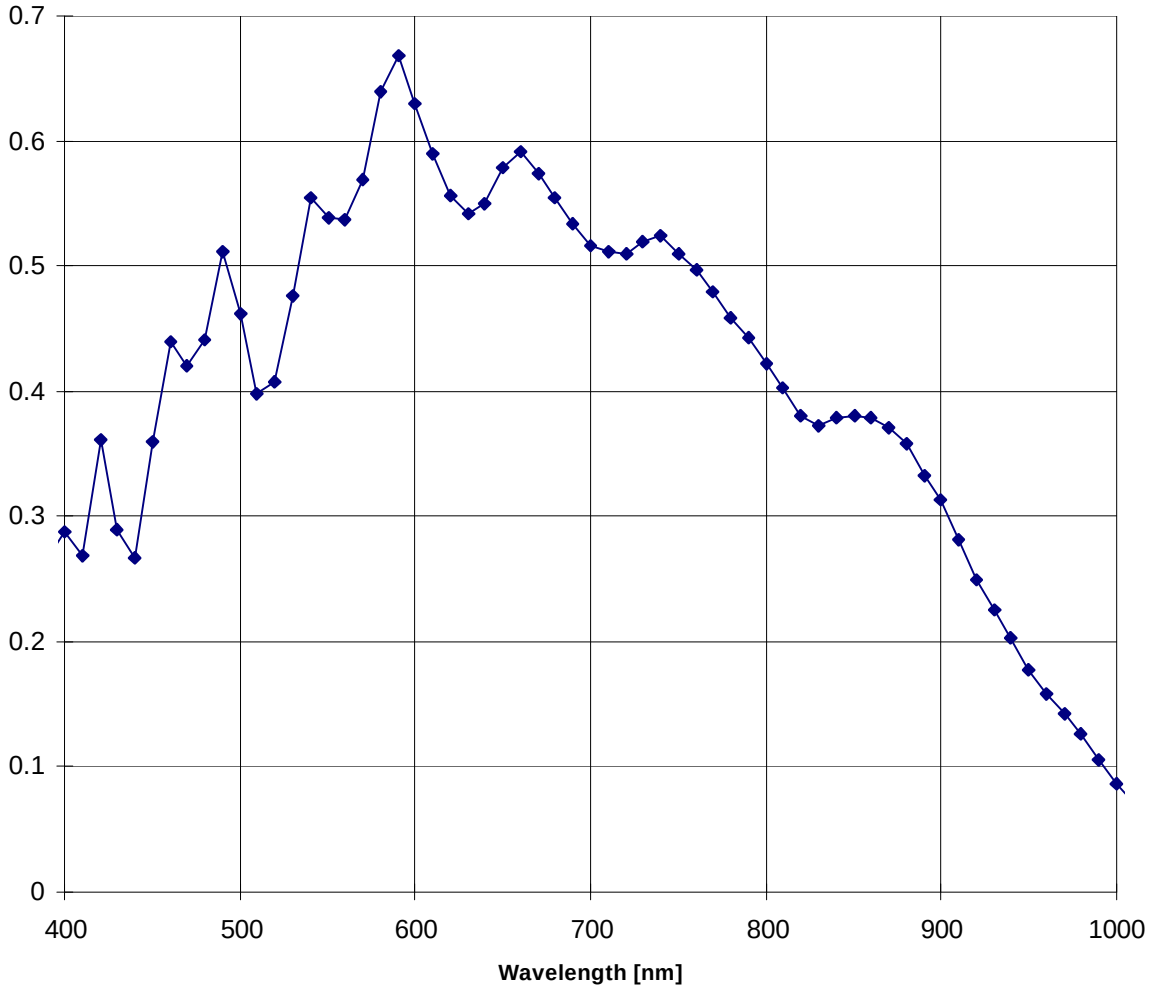


Figure 6 - Typical Spectral Response

Eastman Kodak Company – Image Sensor Solutions - Rochester, NY 14650-2010
Phone (716) 722-4385 Fax (716) 477-4947
Web: www.kodak.com/go/ccd E-mail: ccd@kodak.com

APPENDIX

Appendix 1 – Part Number Availability:

Device Name	Part Number	Features
KAF-0261E	2H4189	Monochrome, Non-LOD, Sealed MAR Cover Glass, Class 0
KAF-0261E	2H4190	Monochrome, Non-LOD, Sealed MAR Cover Glass, Class 1
KAF-0261E	2H4468	Monochrome, Non-LOD, Sealed MAR Cover Glass, Engineering Grade
KAF-0261E	2H4469	Monochrome, Non-LOD, Sealed MAR Cover Glass, Mechanical Grade
KAF-0261E	2H4192	Monochrome, Non-LOD, Snap-On Lid, Class 0
KAF-0261E	2H4193	Monochrome, Non-LOD, Snap-On Lid, Class 1
KAF-0261E	2H4470	Monochrome, Non-LOD, Snap-On Lid, Engineering Grade
KAF-0261E	2H4471	Monochrome, Non-LOD, Snap-On Lid, Mechanical Grade
KAF-0261EU	2H4698	Monochrome, Non-LOD, UV Enhanced, Snap-On Lid

Eastman Kodak Company – Image Sensor Solutions - Rochester, NY 14650-2010
Phone (716) 722-4385 Fax (716) 477-4947
Web: www.kodak.com/go/ccd E-mail: ccd@kodak.com